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NR 251-029-10

GaAs MONOLITHIC MICROWAVE SUBSYSTEM TECHNOLOGY BASE

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December 1980

Final Technical Report for Period 1 April 1979 — 31 May 1980

Approved for Public Release; Distribution Unlimited.

Prepared for

DEFENSE ADVANCED RESEARCH PROJECTS AGENCY
1400 Wilson Boulevard
Arlington, Virginia 22209

OFFICE OF NAVAL RESEARCH
800 North Quincy Street
Arlington, Virginia 22217

UNCLASSIFIED

SECURITY CLASSIFICATION OF THIS PAGE (When Data Entered)

12 152

REPORT DOCUMENTATION PAGE

READ INSTRUCTIONS BEFORE COMPLETING FORM

1. REPORT NUMBER: NR 251-029-3
2. GOVT ACCESSION NO.: AD A103840
3. RECIPIENT'S CATALOG NUMBER:

4. TITLE (and Subtitle): GaAs Monolithic Microwave Subsystem Technology Base
A083613

5. TYPE OF REPORT & PERIOD COVERED: Final Technical rept. 10/79 - 7/80 15 Mar 78-31 May 80

6. PERFORMING ORG. REPORT NUMBER: 81-0571

7. AUTHOR(s): J.G. Oakes M. Cohn; J.E. Degenford M.C. Driver; R.G. Freitag

8. CONTRACT OR GRANT NUMBER(s): N00014-78-C-0268 DARPA Order-3543

9. PERFORMING ORGANIZATION NAME AND ADDRESS
Westinghouse DESC
Systems Development Division
Baltimore, Maryland 21203

10. PROGRAM ELEMENT, PROJECT, TASK AREA & WORK UNIT NUMBERS
61101E/8D10
DARPA order-#3543

11. CONTROLLING OFFICE NAME AND ADDRESS
Defense Advanced Research Projects Agency
1400 Wilson Blvd.
Arlington, Virginia 22209

12. REPORT DATE: Dec 1980

13. NUMBER OF PAGES:

14. MONITORING AGENCY NAME & ADDRESS (if different from Controlling Office)
Office of Naval Research
Code 427
Arlington, Virginia 22217

15. SECURITY CLASS. (of this report): UNCLASSIFIED

15a. DECLASSIFICATION/DOWNGRADING SCHEDULE: N/A

16. DISTRIBUTION STATEMENT (of this Report)

Approved for public release; distribution unlimited.

17. DISTRIBUTION STATEMENT (of the abstract entered in Block 20, if different from Report)

18. SUPPLEMENTARY NOTES

Scientific Officer Telephone: (202) 696-4128

19. KEY WORDS (Continue on reverse side if necessary and identify by block number)

Gallium Arsenide
Monolithic
FET
Integrated Circuits
Ion Implantation
Lithography

20. ABSTRACT (Continue on reverse side if necessary and identify by block number)

During this reporting period, the effort was primarily directed toward increasing the power output per unit of gate width and exploiting the previously developed direct selective ion implantation technology to design, fabricate and evaluate successive iterations of multistage monolithic power amplifiers.

Improvements in GaAs materials and FET device design and processing have resulted in increases in FET output power per

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405897

20. ABSTRACT (Continued)

unit of gate width. Values of 0.7 watts per mm have been achieved, (typical values between 0.6 and 0.7 watts per mm). A device power output of 1.6 watts CW has been measured for an eight cell 2400 μ gate width FET.

The design of wide-band multistage power amplifiers, that observe area conserving constraints necessary for economical monolithic fabrication, is a formidable task. An analysis and optimization procedure which solves this problem has been developed and demonstrated by the design of a wide-band two-stage monolithic power amplifier that yielded a power output of 28 dBm $\pm$0.7 dB over the frequency range from 5.7 to 11.0 GHz. Power outputs of greater than 30 dBm have been achieved over narrower bandwidths.

81-0571

GaAs MONOLITHIC MICROWAVE SUBSYSTEM TECHNOLOGY BASE

WESTINGHOUSE DEFENSE AND ELECTRONIC SYSTEMS CENTER
Systems Development Division
Baltimore, Maryland 21203

FINAL REPORT
March 15, 1978 - May 31, 1980

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M.C. Driver, R.G. Freitag, D.C. Boire

Prepared for:

DEFENSE ADVANCED RESEARCH PROJECTS AGENCY
Contract No. N00014-78-C-0268
DARPA Order No. 3543

Contract Authority: NR 251-028

Effective Date of Contract: March 15, 1978
Expiration Date of Contract: May 31, 1980

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1. INTRODUCTION AND MANAGEMENT SUMMARY

The earlier portions of this program[1] concentrated on:

a. developing the basic technology required for direct selective ion implantation (DSI^2) into unbuffered semi-insulating GaAs wafers,

b. evaluation and use of GaAs wafers made from high purity boules grown under internally funded program at Westinghouse in our Melbourn Liquid Encapsulated Czochralski (LEC) crystal growth facility,

c. power FET design, fabrication and evaluation,

d. increasing FET power output per unit of gate width,

e. analysis of the relationship of amplifier gain and bandwidth on FET power per unit gate width,

f. development of passive lumped constant circuit element design and fabrication procedures,

g. preliminary monolithic power amplifier design and development, and

h. initial 3-bit lumped element phase shifter investigation.

These necessary preliminary efforts set the stage for the results achieved during the remaining portion of this program (October 1, 1979 to May 31, 1980).

During this latter reporting period, the effort was primarily directed toward increasing the power output per unit of gate width and exploiting the previously developed technology to design, fabricate and evaluate successive iterations of multistage monolithic power amplifiers.

Improvements in GaAs materials and FET device design and processing have resulted in increases in FET output power per unit of gate width. Values of 0.7 watts per mm have been achieved

(typical values between 0.6 and 0.7 watts per mm). A device power output of 1.6 watts CW has been measured for an eight cell 2400 μ gate width FET.

The design of wide-band multistage power amplifiers, that observe area conserving constraints necessary for economical monolithic fabrication, is a formidable task. An analysis and optimization procedure which solves this problem has been developed and demonstrated by the design of a wideband two stage monolithic power amplifier that yielded a power output of 28 dBm $\pm$0.7 dB over the frequency range from 5.7 to 11.0 GHz. Power outputs of greater than 30 dBm have been achieved over narrower bandwidths. This powerful design procedure is particularly important for the design of wideband power amplifiers. In hybrid MIC power amplifier design, where area constraints are not usually important, many of the problems can be circumvented through the use of pairs of balanced amplifiers with quadrature hybrid junctions, e.g., Lange couplers, at both the input and output of each stage. This new design procedure, which is described in detail in section 3.3, can be extended to higher power and wider bandwidth amplifiers.

During the approximately two-year duration of this program, many management decisions which affected the program's direction and results were made. Two of them were particularly significant with regard to their impact on the program.

The first was the decision to employ direct selective ion implantation into unbuffered wafers. The then predicted potential advantages were numerous and have been previously described.[1] The immediate impacts were (1) a temporary program slowdown while the necessary technology was refined, and (2) an RF performance degradation due to the lower mobilities initially achievable with commerically available unbuffered chrome doped semi-insulating GaAs wafers. That problem was subsequently eliminated and our

decision was vindicated when our own supply of high purity LEC grown GaAs became available for this program.

The second major decision was to not attempt to incorporate all of the required design features and processing technologies initially. There was concern that to do so would require very complex processing steps too early in the program with the resultant probability of vanishingly small yields of good chips. That in turn would result in untenable delays in evaluating the the many successive signle and multistage design iterations. Examples of necessary and/or desired technologies which were not initially employed are FET and circuit vias, air bridges and thin film capacitors. Each of these technologies were separately studied and developed in a manner that would make their incorporation compatible with the other process steps. The use of vias is an example of a technology which has been incorporated in our monolithic amplifiers. The air bridge and thin film technologies will be incorporated in future monolithic amplifier runs.

Acknowledgement is due to various members of the faculty and staff of Cornell University for their contribution to this program. Professor L.F. Eastman's contributions included:

1. Deep Level Transient Spectroscopy (DLTS) of Westinghouse implanted GaAs wafers which showed very low residual damage levels (Published),

2. Power FET design criteria including gate recess, doping, electrode spacings, predicted output powers (Published), and

3. Analytic model of FET used for quick calculations of expected dc device characteristics.

Professor Eastman and Dr. D.W. Woodard provided significant information on furnace and temperature profile requirements which are important to ohmic contact technology. They also provided important information on etches for both gate recess and cleaning operations that enabled us to improve device fabrication. The

titles of abstracts of two relevant papers written by the Cornell group are included in Appendix G. Professor Walter H. Ku assisted by Mr. Louis C.T. Liu provided sample two-stage amplifier designs based on our small signal FET models which were modified to approximate large signal conditions. Actual two-stage amplifier designs, however, were based on the more accurate procedure discussed in section 3.3 which utilizes experimentally measured load pull characteristics as the fundamental design data.

2. DEVICE FABRICATION

In Appendix B is included the text of a paper approved for publication in a forthcoming IEEE Electron Devices Transactions. The paper contains some of the items reported in the main body of this report but it also includes some improvements in gain obtained by polishing the back of the wafer instead of merely lapping it.

2.1 MATERIAL GROWTH

During this program a great deal of success has been achieved in the growth of high purity, two and three-inch diameter <100> GaAs crystals pulled from pyrolytic boron nitride crucibles. The growth of of these crystals is described in some detail in Appendix A but it is worthy of note that resistivities after thermal annealing in the high 10^7 ohm cm range have been achieved in undoped gallium arsenide pulled from pyrolytic boron nitride.

2.2 ION IMPLANTATION

The techniques and results of ion implantation were fully covered in the first year's report on this program.(MD-1) Since that time, some progress has been made in the quantitative assessment of the work.

A major effort has been directed toward increased understanding of activation and mobility in ion implanted GaAs. This was made possible by the greatly improved uniformity and reproducibility achieved in LEC GaAs grown from pyrolytic boron nitride. The most significant result is that the activation efficiency (η) typically quoted to characterize

$$\eta = N_D^+ - N_A^- = \frac{N_D^+ - N_A^-}{N_I} N_I = \eta' N_I$$

where η is the free carrier concentration which equals the net donor concentration and N_I is the implanted ion concentration. Both are inadequate and misleading. Implantations are now characterized by the relationship

$$\eta = N_D^+ - N_A^- = \left\{ \frac{N_D^+ - N_A^-}{N_D^+ + N_A^-} \right\} \left\{ \frac{N_D^+ + N_A^-}{N_I} \right\} N_I = \eta_\Delta \eta_\Sigma N_I$$

$$\eta = \eta_\Delta \eta_\Sigma$$

$$\eta_\Sigma = \frac{N_D^+ - N_A^-}{N_I}$$

$$\eta_\Delta = \frac{N_D^+ - N_A^-}{N_D^+ + N_A^-}$$

where the total ionized impurity concentration of implanted layers $(N_D^+ + N_A^-)$ is evaluated by detailed analysis of the mobility at 300^oK or 77^oK. 100% activation efficiency (η_Σ) is achieved if allowance is made for approximately 1×10^{16} / cm^3 residual acceptors and pairing of implanted donors with Cr acceptors. η_Δ values of approximately 75% are achieved for 860^oC anneals of Si^{29} implants; this appears to be a thermodynamic limit rather than a process or substrate limit. It is found that blind attempts to achieve η = 100% results in $\eta_\Sigma > 100\%$ and an ionized impurity concentration that cannot be rationalized, or in principle controlled, with the implanted ion concentration.

2.3 FABRICATION PROCEDURE

The use of SiO_2 to assist in the definition by lift-off of the metal layers was discontinued as noted in the previous report. The most recent fabrication procedure is as follows.

Wafers are cut from boules grown by the liquid encapsulated Czochralski process. In many cases, these boules are ground to a diameter of 2" with two <110> flats to establish the orientation of the wafers. The wafers are lapped and polished to a

thickness of 25 mils before being selectively implanted with silicon (^{29}Si) using the procedure shown in figure 2-1.

The "front" surface of the gallium arsenide is covered with 1000Å of silicon nitride which is deposited using a plasma-enhanced chemical vapor deposition system which dissociates nitrogen and silane to produce the insulator. 2500Å of 7% phosphorus-doped silicon dioxide (PSG) is deposited on top of the Si_3N_4 using a CVD reactor. A pattern is formed in AZ1350J photoresist and the SiO_2 is etched down to the Si_3N_4 to form the ion implantation mask. ^{29}Si ions are implanted through the Si_3N_4 as shown in figure 2-1(A).

The photoresist is then removed and a second 2500 A thick layer of PSG is deposited as shown in figure 2-1(B). The phosphorus doping is employed to ensure that this glass becomes plastic at the 860°C annealing temperature and does not lead to stress damage associated with differences in thermal expansion coefficients. It is also an essential element in the registration of selective implants and prevents pit formation at pinholes in the primary Si_3N_4 encapsulation.

The wafers are annealed in a forming gas (10% hydrogen 90% nitrogen) atmosphere using ramping of the wafer into a furnace such that the wafers rise from room temperature to 860°C in 20 minutes. Their temperature holds at 860°C for 15 minutes and then falls back to 25°C in 25 minutes. The furnace contains a flat zone 2-1/2" wide and 8" long.

After the annealing step, alignment marks are formed in the gallium arsenide using ion milling as shown in figure 2-1(C) using a further layer of photoresist as a coarse mask. The PSG that was used as part of the first ion implantation mask provides the mask for the area ion milled into the gallium arsenide surface. This area is therefore, automatically and precisely aligned with the implanted area.

At the center of each wafer is a square area that is uniformly implanted with ions to provide an evaluation capability for the

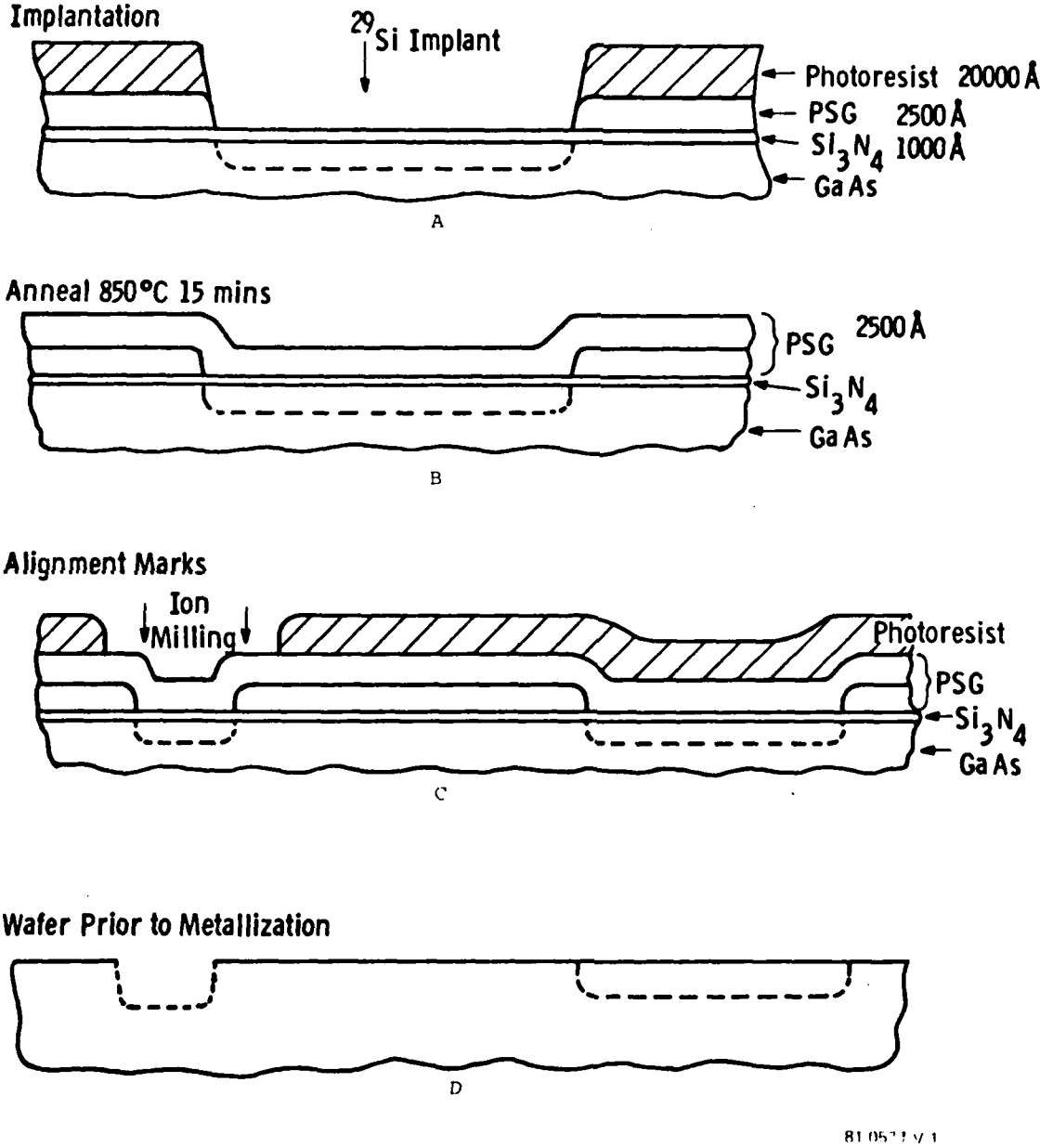


Figure 2-1. Implantation and Alignment Mark Fabrication

implant. After the implantation, an aluminum dot pattern is formed on this square which allows C-V measurements to be made. It is important at this stage of the device development to know in detail the quality of the implant and activation.

2.3.1 Wafer Metallization

After evaluation, the aluminum dots and the remaining PSG and Si_3N_4 are removed and the wafer is ready for the source-drain ohmic contact metallization which consists of gold-geranium alloy 1200 Å) followed by nickel (500 Å) and platinum (400 Å). When alloyed to a peak temperature of 500°C in forming gas this metal system has consistently produced specific contact resistances less than $3 \times 10^{-6} \Omega\text{-cm}^2$. The metal is defined by a lift-off process using AZ1350 photoresist 1 μm thick. A schematic cross section of the ohmic metallization prior to lift-off is shown in figure 2-2. In order to assist the lift-off process, the photoresist is treated with chlorobenzene in the manner described later in this process review.

After alloying of the source-drain metallization, the gate pattern is defined, again using AZ1350 photoresist 1 μm thick as shown in figure 2-2. Prior to deposition of the gate metal, the exposed gallium arsenide surface is etched up to 1000 Å to form a recess into which the gate is deposited.(MD2) The metals evaporated are titanium (500 Å), platinum (500 Å) and gold (4500 Å). The gate is offset in our present design being spaced 1.5 μm from the source contact and 3.5 μm from the drain contact in order to minimize the source resistance while maintaining adequate gate-drain spacing to avoid premature breakdown at the drain edge.MD3 The metal is again defined by a lift-off process involving chlorobenzene treatment. A scanning electron micrograph of a completed FET is shown in figure 2-3. The gate length is 1 μm and this micrograph clearly indicates the clean quality of the gate metallization.

The final metallization on the front of the surface of the wafer is the circuit metal which consists of chromium (800 Å),

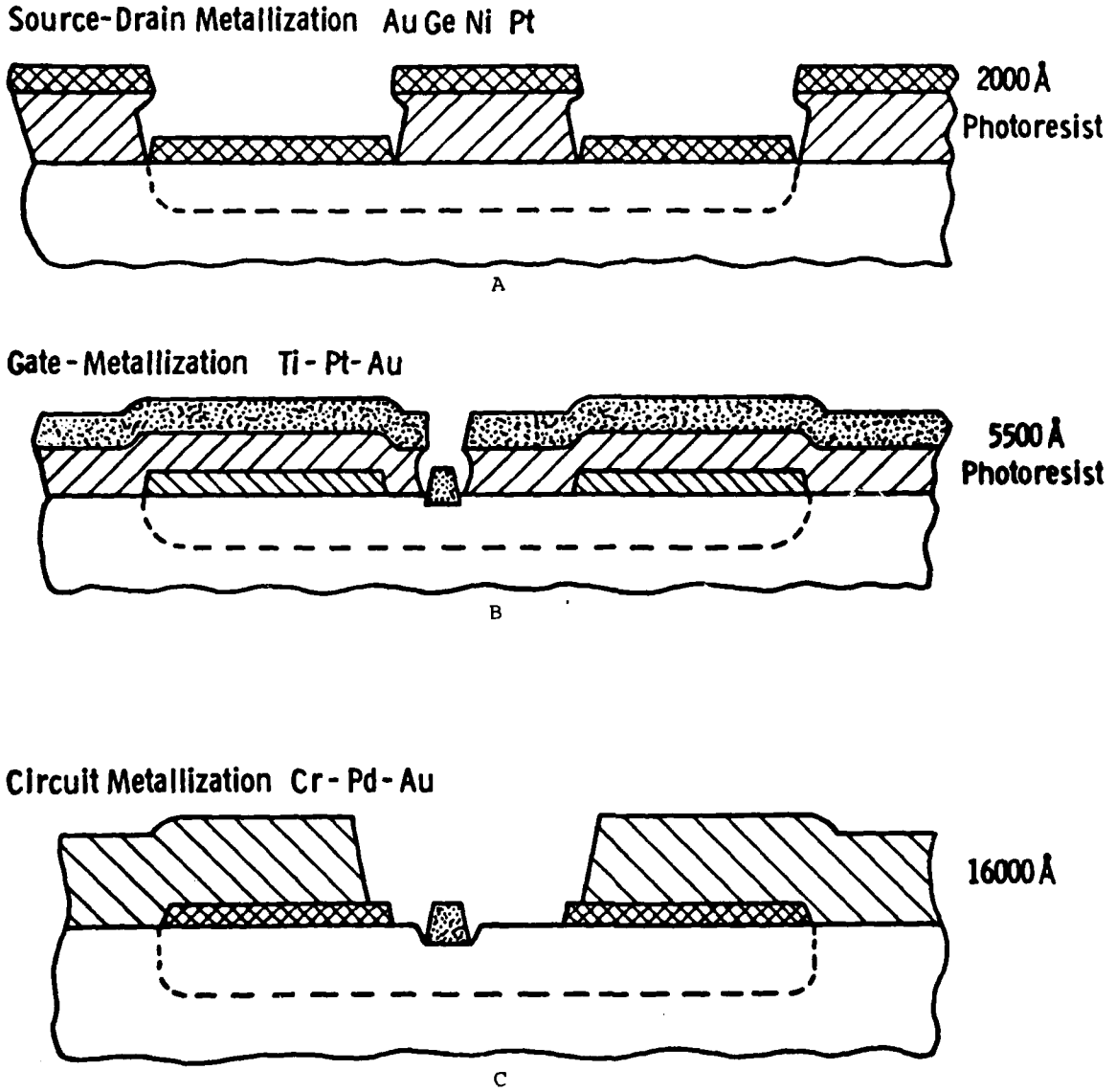


Figure 2-2. Metallization of Contacts and Circuit

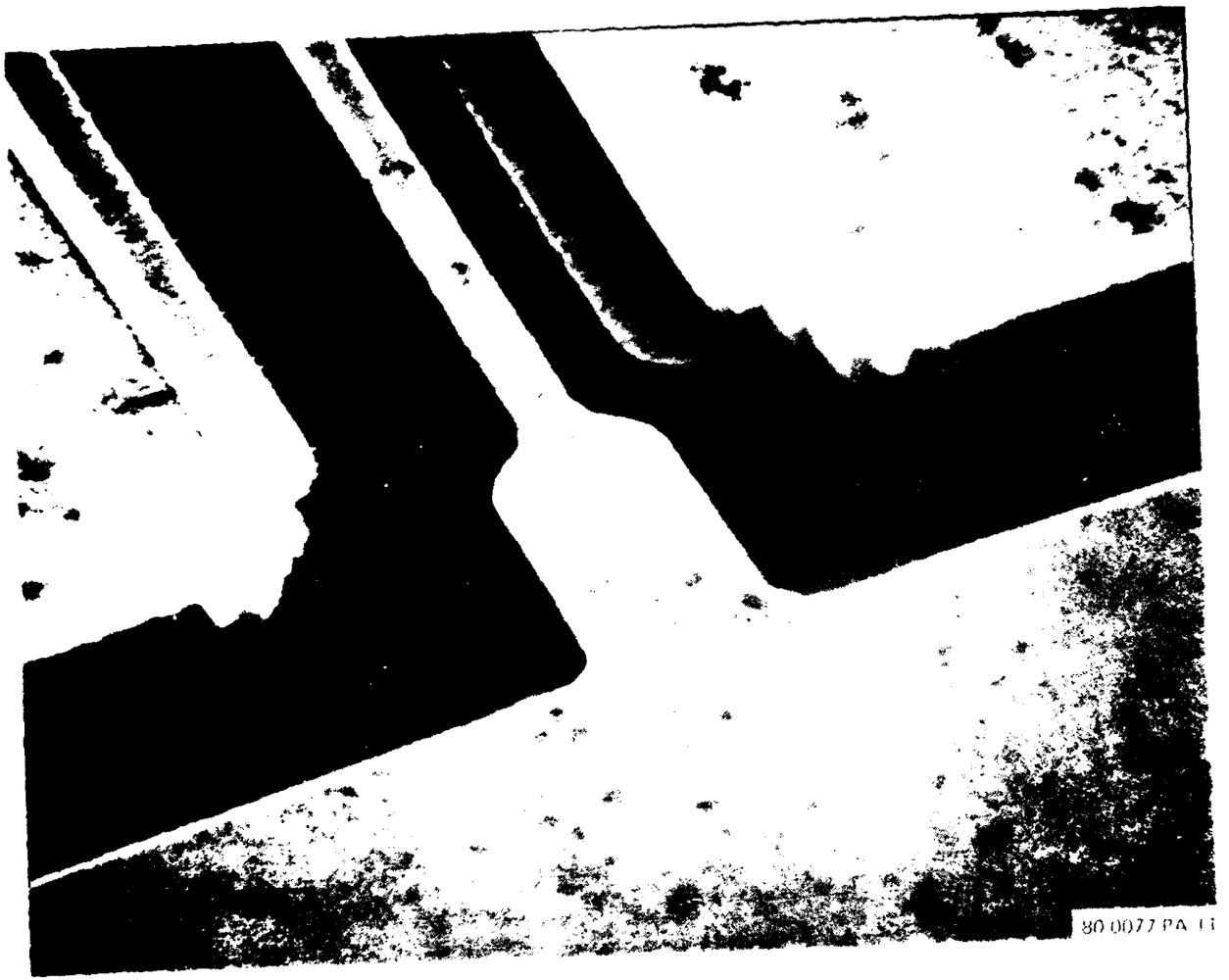


Figure 2-3. FET Fabricated Using the Chlorobenzine Process

palladium (100 Å) and gold 19,000 Å). This amount of metal is the minimum necessary since at the lowest frequency of interest (5 GHz) the skin depth in gold is 1.1 μm. The ohmic contacts are also partially covered with this thick metal to reduce their spreading resistance (see figure 2-2).

The chlorobenzene treatment[MD4] mentioned earlier is again used for the photoresist defining the circuit metallization. A schematic diagram of the chlorobenzene process is shown in figure 2-4. After exposure of the AZ1350J photoresist and before development, the photoresist is soaked for 6 minutes in chlorobenzene at room temperature. The action of the chlorobenzene is to form a hardened crust on the surface such that after development a lip is formed which causes a break in the metal that is subsequently evaporated. A scanning electron micrograph of a 1 μm thick AZ1350J photoresist is shown in figure 2-5.

2.3.2 Wafer Thinning and Metallization

When the circuit metallization is completed the wafer is mounted onto a lapping block and the back surface lapped with 1 μm alumina lapping compound until the wafer is 150 μm thick. A bromine methanol polish is then used to reduce the final thickness to 100 μm. The wafer is then removed from the lapping block and mounted on a glass plate where the pattern for the etching of the via connections through the wafer is defined. The fabrication of the vias will be discussed in more detail later.

Upon completion of the via etch, titanium (500 Å) gold (10,000 Å) is sputtered on the back surface of the wafer to metallize the inside of the via holes and to provide a ground plane on the back surface of the wafer. After removal from the glass slide the back metal is thickened by the evaporation of chromium (800 Å), gold (10,000 Å), nickel (500 Å) and gold (2000 Å). The function of the nickel is to provide a barrier against the gold-tin alloy that is used to solder the device chip to the microwave header.

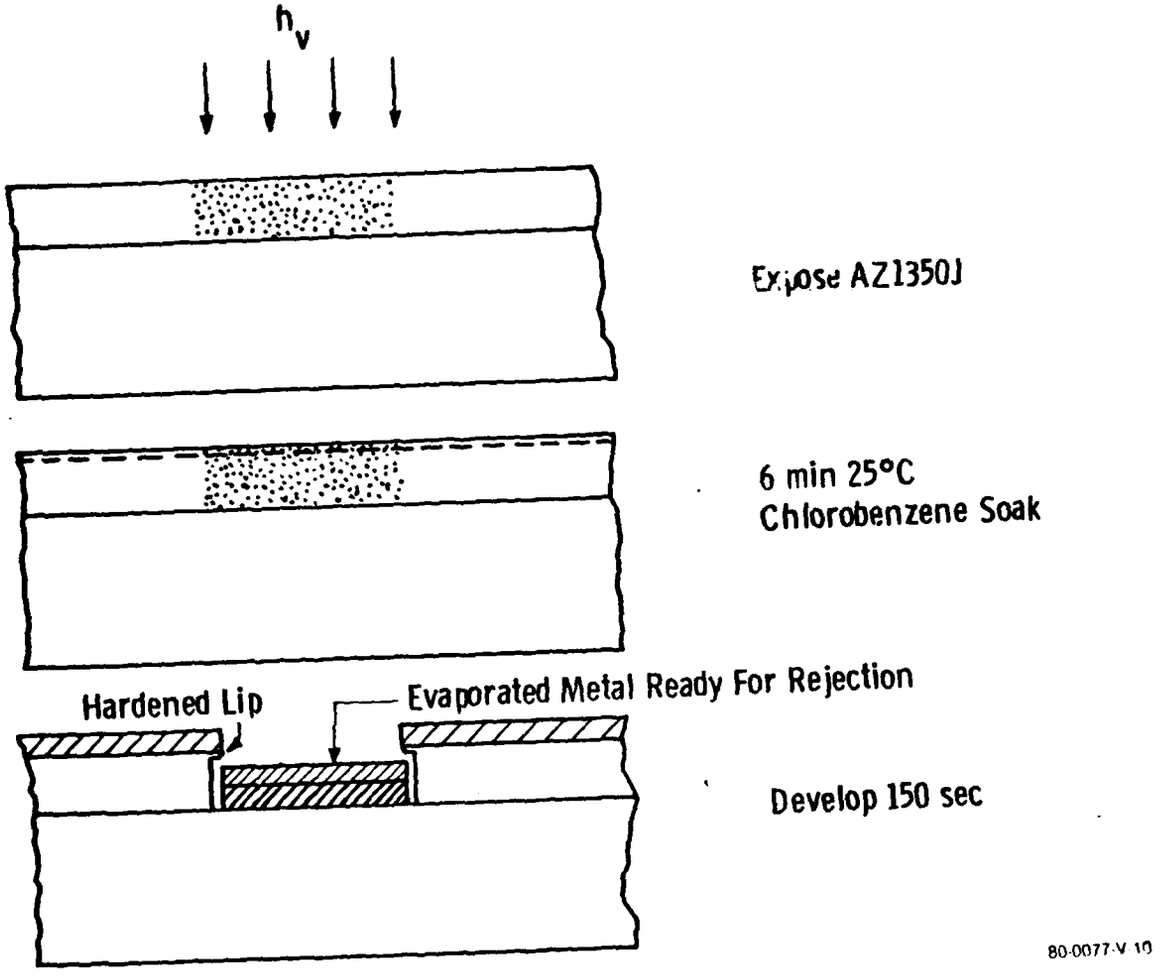


Figure 2-4. Schematic Diagram of the Chlorobenzene Photoresist Process

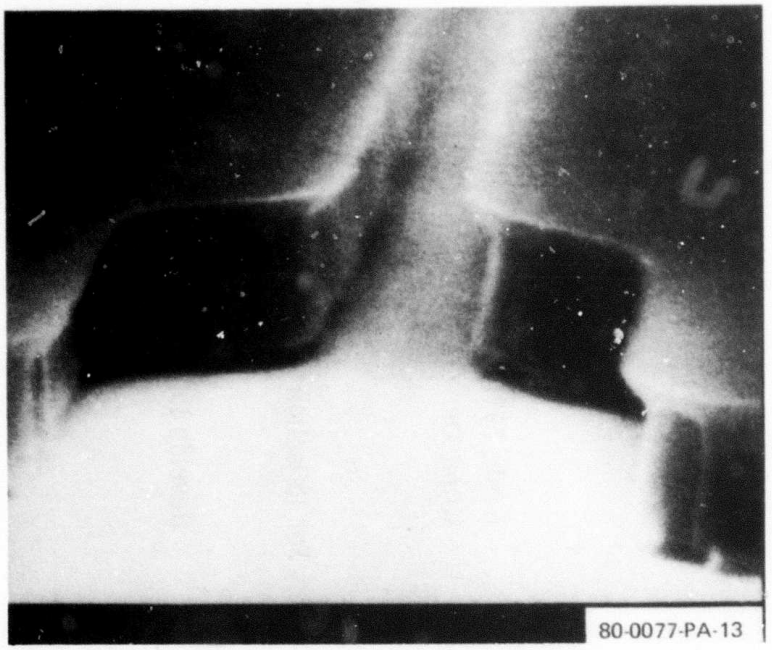


Figure 2-5. SEM of 1 μm Gate Opening in 1 μm Thick Chlorobenzene Treated Unit

The wafer is then mounted face up onto a glass slide for separation of the individual chips by sawing with a 1-1/2 mils thick diamond saw. They are then thoroughly cleaned before being dc tested by probing.

Those chips showing good dc characteristics are soldered to chip carriers designed to provde 50 Ω input and output microstrip lines, bias lines and places for the bypass capacitors that are presently mounted externally to the chip.

2.3.3 Via Technology

Vias have been used successfully in discrete FET's[4] to make connections between the source contacts of the FET's and the ground plane on the back of the gallium arsenide wafer. The design of our amplifiers is based on a microstrip approach where the width of the conductors and the thickness of the semi-insulating substrate defines the inductance of the interconnecting lines. The thickness of the gallium arsenide is chosen to be 100 μm to give acceptable losses in the circuitry. With this

thickness the problems of fabricating vias are more acute than for the 30 μm thick substrates used by other workers. We have used two approaches.

In the first approach a large area "tub" is first etched in the back of the gallium arsenide wafer aligned to the area of the whole FET using infrared alignment and photoresist masking. Subsequently an additional layer of photoresist is used to etch holes at the bottom of these tubes to form vias to the source metallization. This is clearly shown in the scanning electron micrographs of figure 2-6. Figure 2-7 shows a circuit with vias to every source pad.

For the second approach the circuit is designed with a few large area vias as shown in figure 2-8. At present, the source pads are interconnected using bond wires. An air bridge technology has been developed but is not yet included in this circuit fabrication.

The advantages of vias is that they improve the gain of the FET by significantly reducing the source inductance and, in addition, they provide great flexibility in the circuit design by allowing RF ground to be achieved readily anywhere on the slice.

2.3.4 Yield

A recent fabrication run (IC20) has shown an excellent yield of circuits under dc testing of FET's, capacitors and via structures. For wafer IC20C the number of circuits with all capacitors and FET's without shorts or opens is 9 out of a total of 46 tested for a yield of 14.6%. For wafer IC21D, this figure is even better with a total of 21 good out of a total of 52 tested or a 40.4% yield. These figures do not include those circuits at the edge of the round wafer that were incomplete.

The reasons for these encouraging figures are several changes made to the fabrication procedure:

1. The mask for the final thick metallization for the circuit was redesigned such that the capacitor fingers are

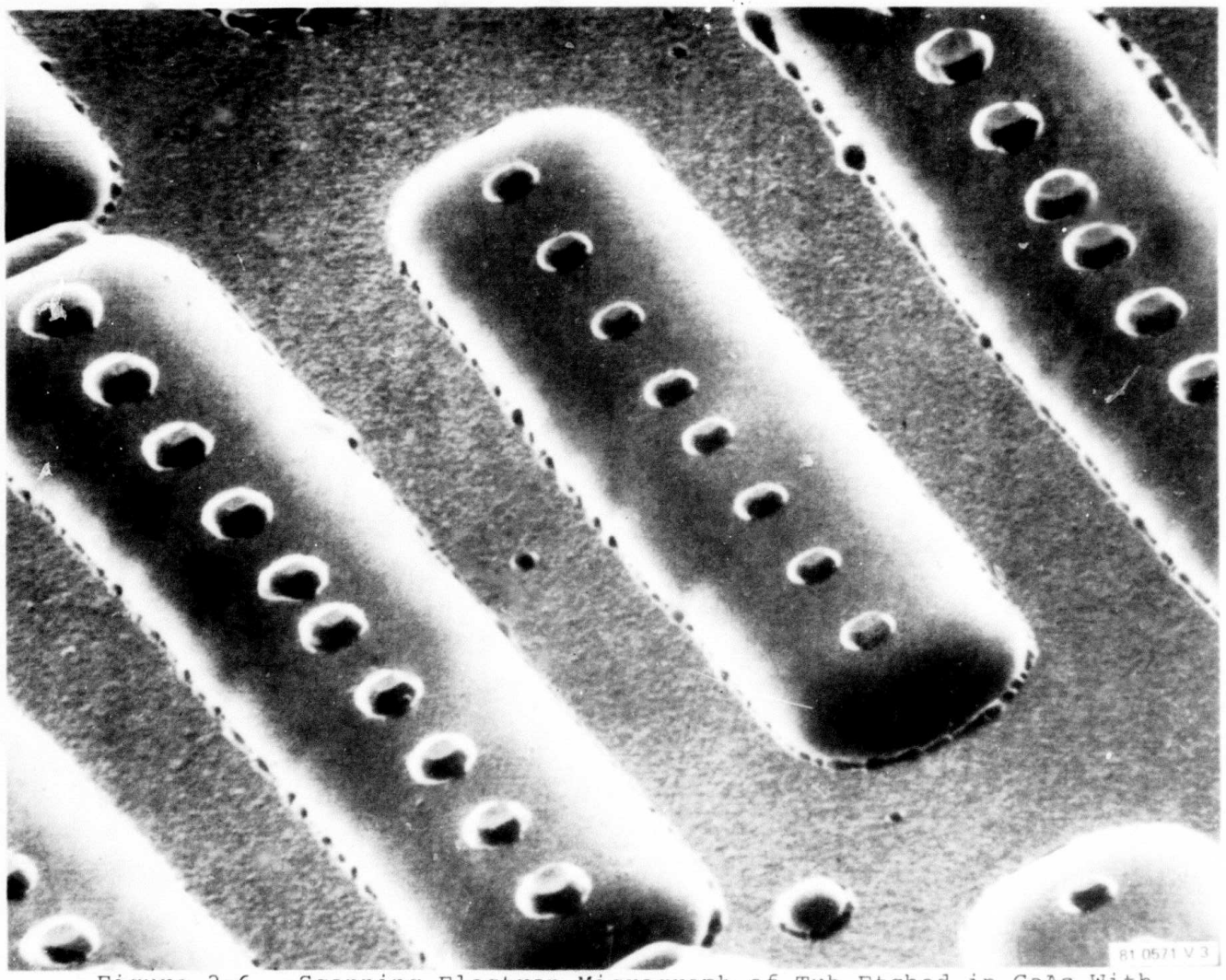


Figure 2-6. Scanning Electron Micrograph of Tub Etched in GaAs With Vias to Every Source at the Bottom of the Tub

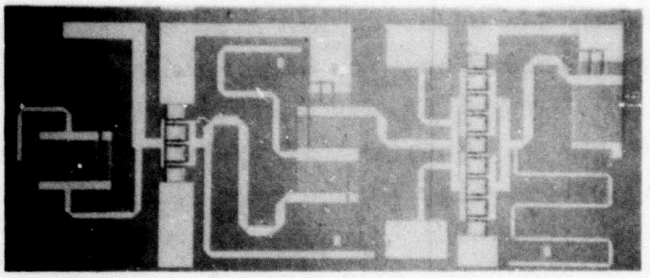


Figure 2-7. Circuit Design With Vias to Every Source

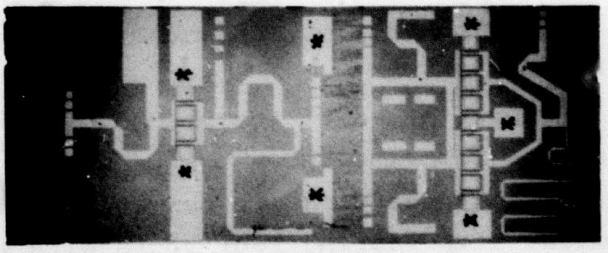


Figure 2-8. Circuit Designed for "Sparse" Via Technology Vias Placed in Areas Marked by Asterisks

parallel to the gate fingers on the FET's. One of the principal causes of failure of the capacitors is the deposition of metal on the side wall of the photoresist used to define the capacitor geometry. This thin layer of metal peels off during lift off of the excess metal and lies across the fingers causing shorts. A similar problem can occur in the area of the gates on the FET's if metal is deposited along the side wall of the photoresist defining the thick metal on the source and drain contact pads. These problems can be minimized if the wafer is oriented with respect to the evaporation source such that the planes defined by the gates, the capacitor fingers and the source are approximately normal to the plane of the wafer. Under these conditions, the amount of metal deposited on the side walls of the long dimension of the capacitors and FET's is a minimum.

2. The design of the interdigitated capacitors is 5 μm wide fingers with 5 μm wide spaces. The fabrication process for the photomasks results in the capacitor fingers being defined at 6 μm with 4 μm spaces. The device fabrication process further changes these dimensions to 7 μm wide fingers with 3 μm spaces. While the changes in the value of capacitance can be compensated for by building in trim capacity, the yield of interdigitated capacitors with just 3 μm spaces is low. The most recent mask design for the circuit metallization has made allowances for the dimension changes during fabrication and hence the yield of the capacitors has improved.

3. The implementation of the second of the two methods for fabricating vias described previously has resulted in fewer failures. In addition, the vias are now being etched in one continuous chemical step lasting four hours with special attention being paid to the removal of bubbles formed in the via holes. The yield of good vias on a wafer now exceeds 99% with one hole bad on a wafer containing 53 circuits with 7 via holes/circuit.

4. The edges of the glass plates on which the wafers are mounted during the etching of the vias have been bevelled to reduce scratching of the metal during removal.

5. The top surface of the wafers are covered with 4-5 μm of AZ1275 photoresist during the lapping process to help protect them against lapping compound scratching and again during the sawing apart of the dice to protect against gallium arsenide particle damage. During this latter step the wafer is also covered with a low melting point wax. AZ1275 is not used on the front surface during the via etching and subsequent metallization due to the danger of overheating the resist during the sputtering of the Ti-Au layer which would thereby make it difficult to remove.

The presence of the photoresist during the final cleaning stages has allowed the removal of the surface wax and the sawing debris by a vigorous trichloroethylene jet. A subsequent soak in acetone has produced very clean chips.

2.4 DISCRETE DEVICE PERFORMANCE

Each fabrication run of circuits contains some discrete devices which are fully evaluated in terms of their S-parameters and power response in order that the next generation of amplifiers may be designed on the basis of these measurements. Accordingly, during the last few months of this contract, the aim has been to keep the discrete device parameters as constant as possible.

2.4.1 Small Signal Response

A typical set of S-parameters from 2 GHz to 12 GHz is plotted on a Smith chart in figure 2-9 for a 1200 μm periphery FET from run IC-7 at V_D = 10 volts, V_G = -2 volts, and a drain current of 197 mA which is about half of I_{DSS}. S_{11} represents a well-behaved series R-L-C circuit with a real part of about 5 ohms. This is typical for a 1200 μm FET. S_{22} is more complex and needs both parallel and series elements to be modelled. The relatively large S_{22}, particularly at the low frequencies indicates a high value of R_{DS}. The S_{12} is less than 0.1 and corresponds to very low reverse feedback through the FET on the header. Finally, S_{21}

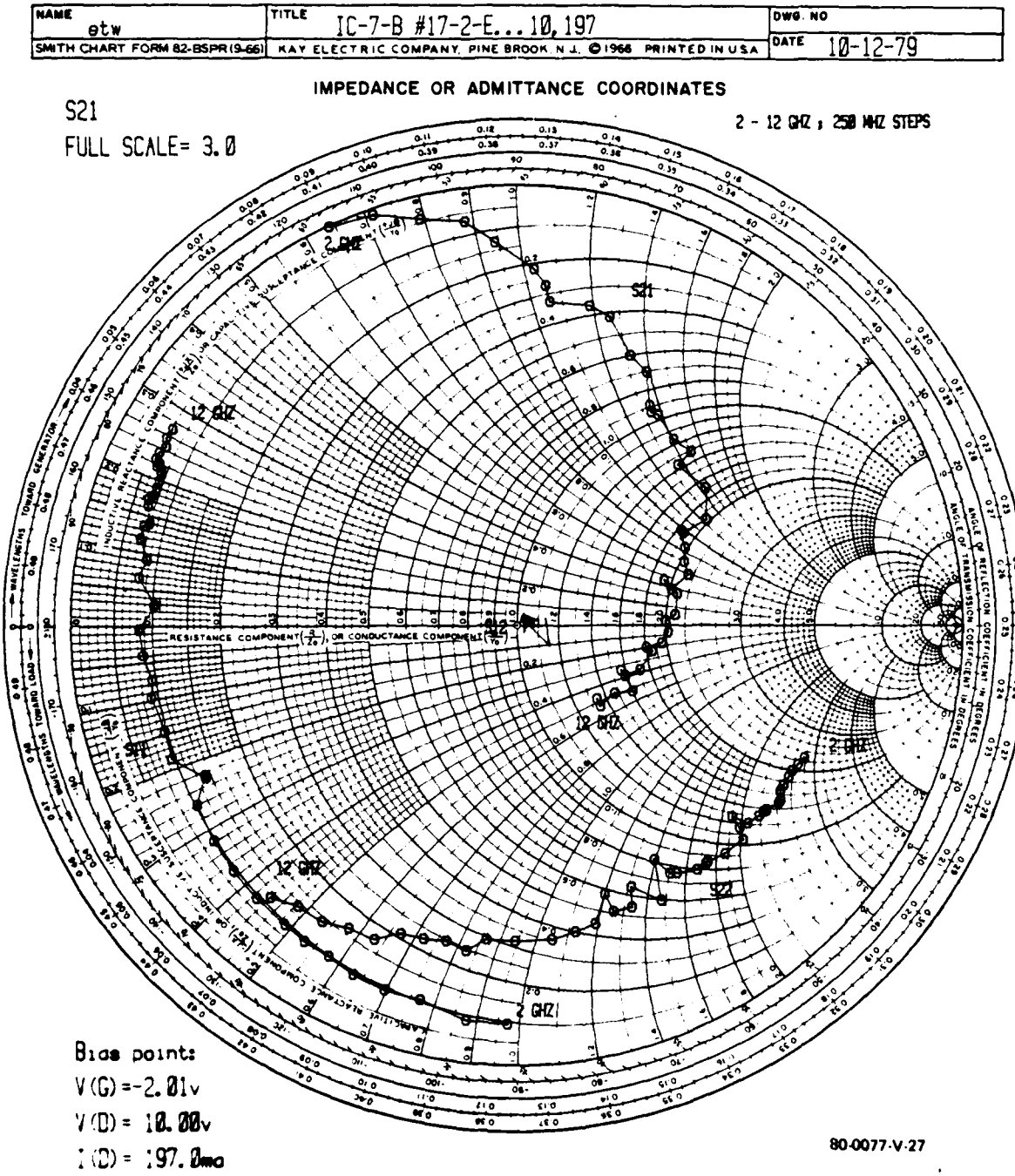


Figure 2-9. S-Parameters for IC7 1200 μm FET

is large. The magnitude at the outside of the Smith Chart is 3.0 for The S_{21} curve. The magnitude of S_{21} drops below 1.0 above 9 GHz. The maximum available gain of our power FET's is 10-12 dB at 8 GHz and 7-10 dB at 10 GHz. These values are calculated from the S-parameters and verified during the power testing of each device.

The small signal S-parameters are used to construct a model of typical devices from each run. This allows us to identify and isolate any device problems which may occur. The model also provides us with input matching data for our IC designs. In general, we observe about 1.0 pF/mm input capacitance, 5Ω-mm series input resistance, 75 to 90 mmhos/mm transconductance and 0.25 pF/mm parallel output capacitance.

2.4.2 Power Response

The best power performance quoted in our last report[MD-1] was 0.64 watts/mm of periphery with 4 dB of gain at 8 GHz. This value has been raised to 0.7 watts/mm for 4 dB of gain at the same frequency for a 900 μm periphery device (IC-10C). The response of the 900 μm periphery FET at 8 GHz is shown in figure 2-10. This device shows a linear gain of over 9 dB in the power tuning mode and produces 27.5 dBm (562 mW) with 7.5 dB of gain corresponding to 0.62 W/mm.

A 2400 μm device from a different run (IC 20B) has delivered only slightly less power/unit periphery (0.657 watts/mm) while delivering 1.58 watts at 8 GHz and 4 dB gain. This device was fabricated on undoped (BN6) gallium arsenide. A plot of the device response is shown in figure 2-11. The small signal gain of 5-8 dB is lower than that of the 900 μm device because of extra loss associated with the source interconnection which was accomplished by hard wires on this run.

The testing of these devices was performed on the automatic test setup described previously.[MD-1]

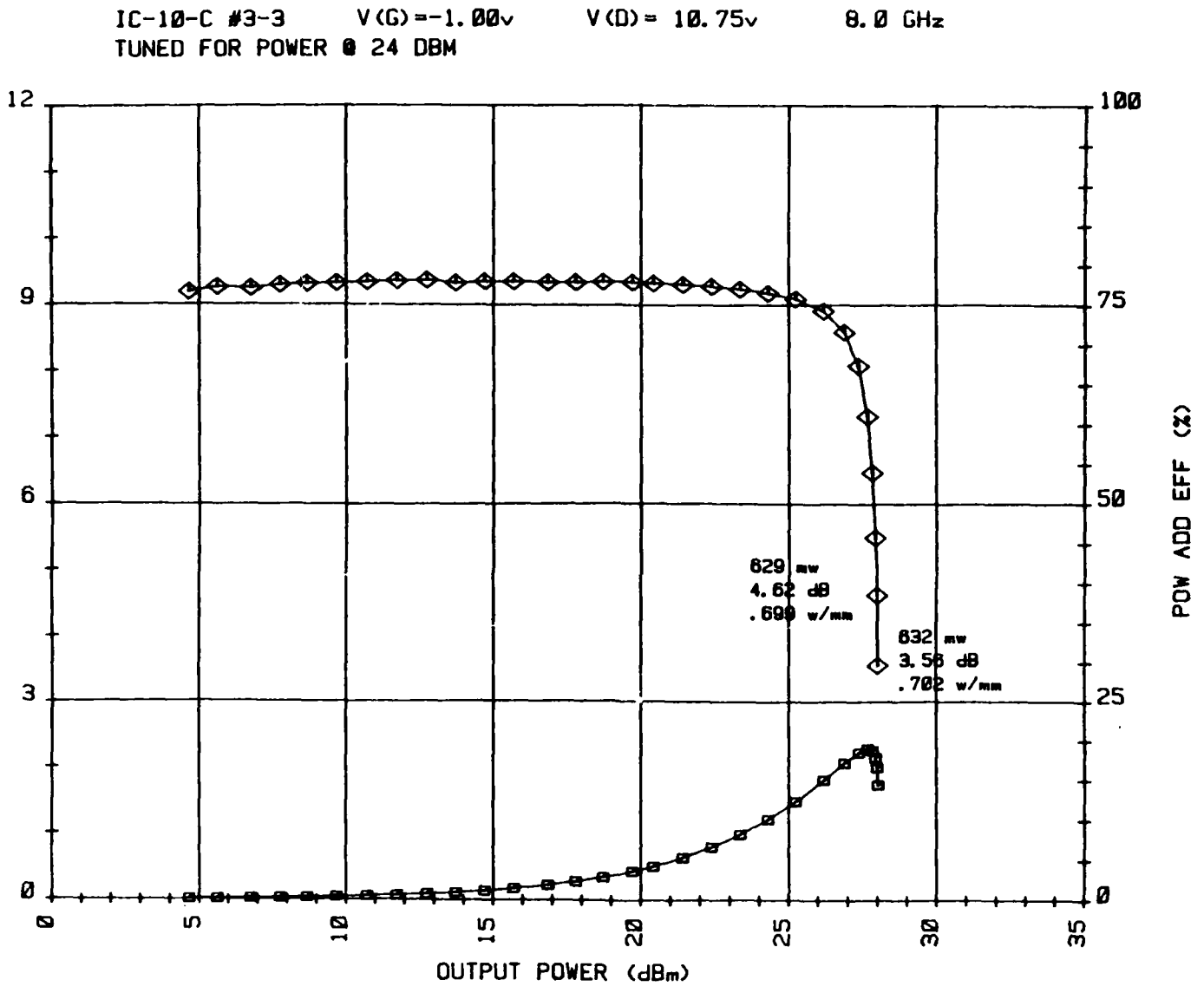


Figure 2-10. Power Output and Gain of a 900 Micron Periphery GaAs FET

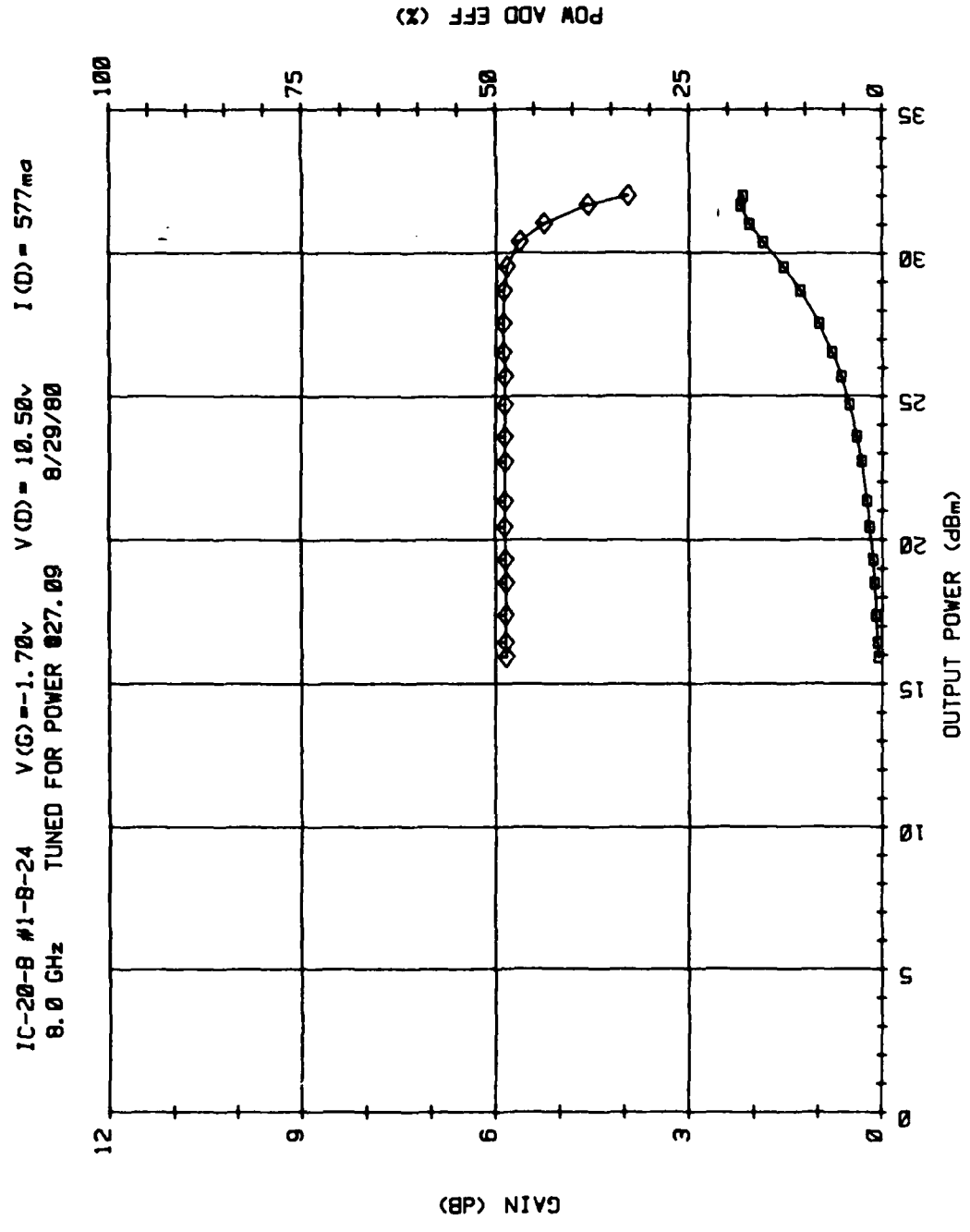


Figure 2-11. Power Output and Gain of 2400 μm Periphery GaAs FET

The power output per unit periphery of the ion implanted FETs fabricated on this contract since October 1978 is shown in figure 2-12. The average power is around 0.6 watts for the last 10 runs, both in lightly chromium-doped and undoped wafers.

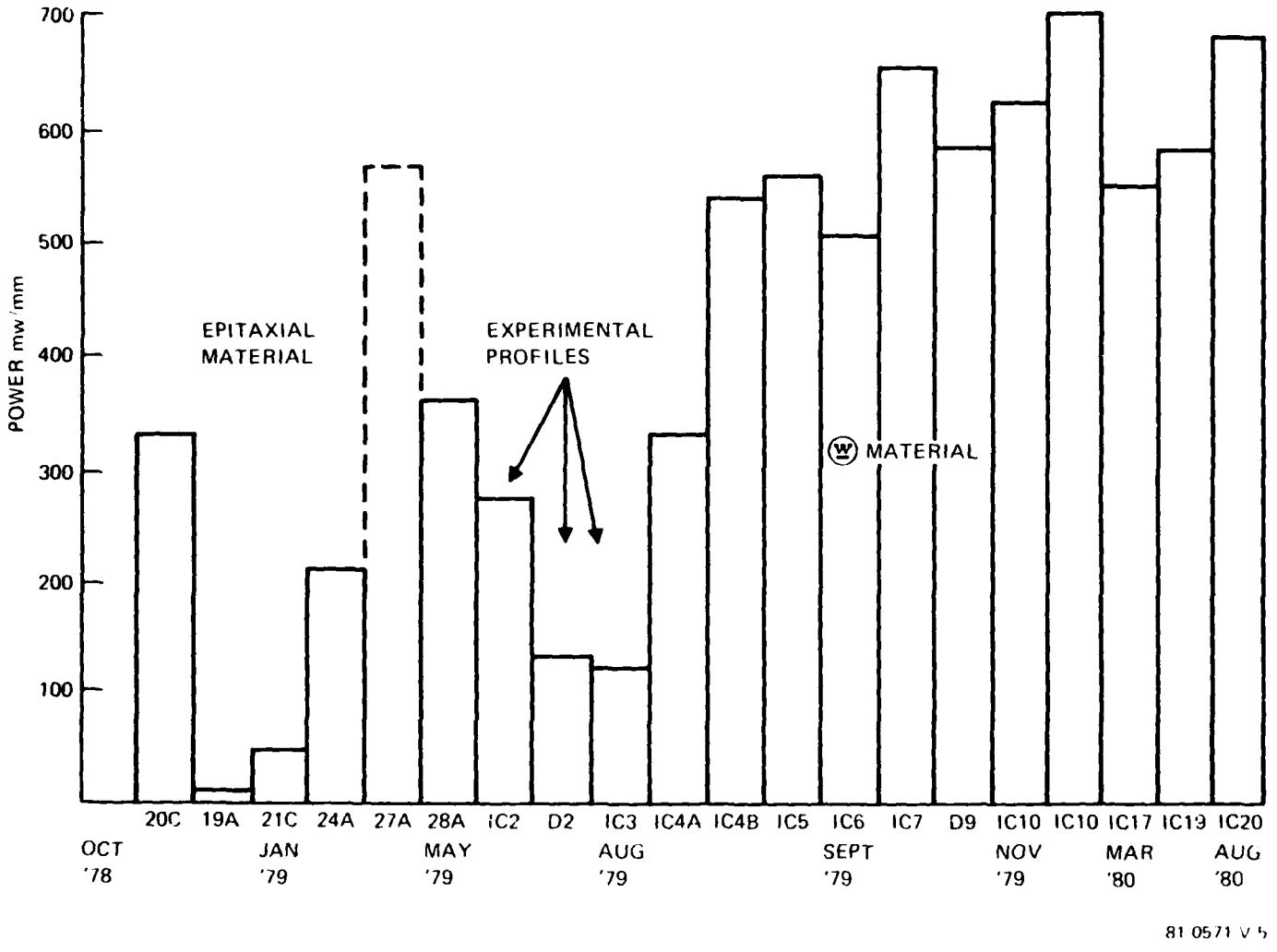


Figure 2-12. Power Output Per Unit Periphery for Westinghouse Ion Implanted FET's Since October 1978

REFERENCES

MD1 J.G. Oakes and J. Degenford, Annual Tech. Report on Contract N00014-78-R-0268

MD2 S. Tiwari et al., IEEE Trans. Elect. Dev., ED-27 (6), June 1980

MD3 R. Yamamoto et al., IEEE Trans. Elect. Dev., ED-25 (6), June 1980.

MD4 B.J. Canavello et al., IBM Tech. Disclosure Bull. 19 (10), March 1977.

3. AMPLIFIER DESIGNS

3.1 INTRODUCTION

During the course of this program, three different monolithic amplifier types have been studied: 1) narrow-band single stage, 2) octave band single stage, and 3) two-stage octave band. The narrow-band designs were used primarily as vehicles for testing discrete FETs and circuit elements and were described in the technical report covering the period September 30, 1978 - September 30, 1979 (NR251-029-10). Hence, only the octave band designs will be discussed here.

Also studied were on-chip circuit trimming techniques which significantly enhanced the understanding and performance of these amplifiers and provided design information for the next design iteration.

One of the major problems encountered in designing wideband multistage FET power amplifiers is achieving the required 6 dB/ octave/stage gain compensation over the band as well as maximum power output simultaneously.

Reactive mismatching is commonly used to provide the required gain compensation, however, the severe mismatches created thereby complicate the design of interstage network considerably.

The interstage circuit has to simultaneously provide:

- Gain Equalization
- Present optimum load impedance to output of proceeding stage (for max. pwr, out.)
- Matching to input of following stage

In hybrid amplifiers, this problem is overcome by routinely using hybrid coupled balanced amplifier pairs for each stage. To implement such an approach requires input and output quarter-wavelength directional couplers plus two parallel gain and phase

matched amplifier stages. For monolithic amplifiers, such an approach is very wasteful of GaAs substrate area, particularly for frequencies below 10 GHz.

An alternate technique has been developed which distributes the gain equalization among input, interstage, and output stages. This alternate approach is based on load-pull characterization of the devices and is discussed in section 3.3. A description of the load-pull measurements is contained in section 3.2.2.

3.2 FET CHARACTERIZATION

3.2.1 S-Parameters and Small Signal Models

For power amplifier designs, FET characterization includes both small signal S-parameters measurements plus the load-pull measurements discussed in the next section. Typical S-parameters for the Westinghouse FET's are shown in figure 3-1. Small signal models derived from these S-parameters are shown in figure 3-2a&b for typical recent Westinghouse 900 and 1200 μ FET's. While the input S-parameters and corresponding input circuit is still appropriate for large signal design, the optimum large signal load impedance must be determined using the load pull measurements discussed in the next section.

3.2.2 Load-Pull Measurements and Amplifier Design Techniques

In order to fully characterize the discrete FETs for subsequent high power amplifier design, it is essential to have data relating output power to FET load impedance. Such "load pull" data as shown in figure 3-3 can be obtained using mechanical tuners, but such a procedure is very time consuming since the setup must be disassembled after each measurement to measure tuner impedance. An alternate "electronic" load-pull setup[1] as shown in figure 3-4 is vastly superior since it allows rapid, accurate measurements and automatic recording of data on a Smith chart.

This type of load-pull setup basically simulates a reflected wave electronically by sampling and amplifying a portion of the

[1] C. Rauscher and H.A. Willing, "Simulation of Nonlinear Microwave FET Performance Using a Quasi-Static Model", IEEE MTTS Trans., Vol. MTT-27, pp. 834-840, October, 1979.

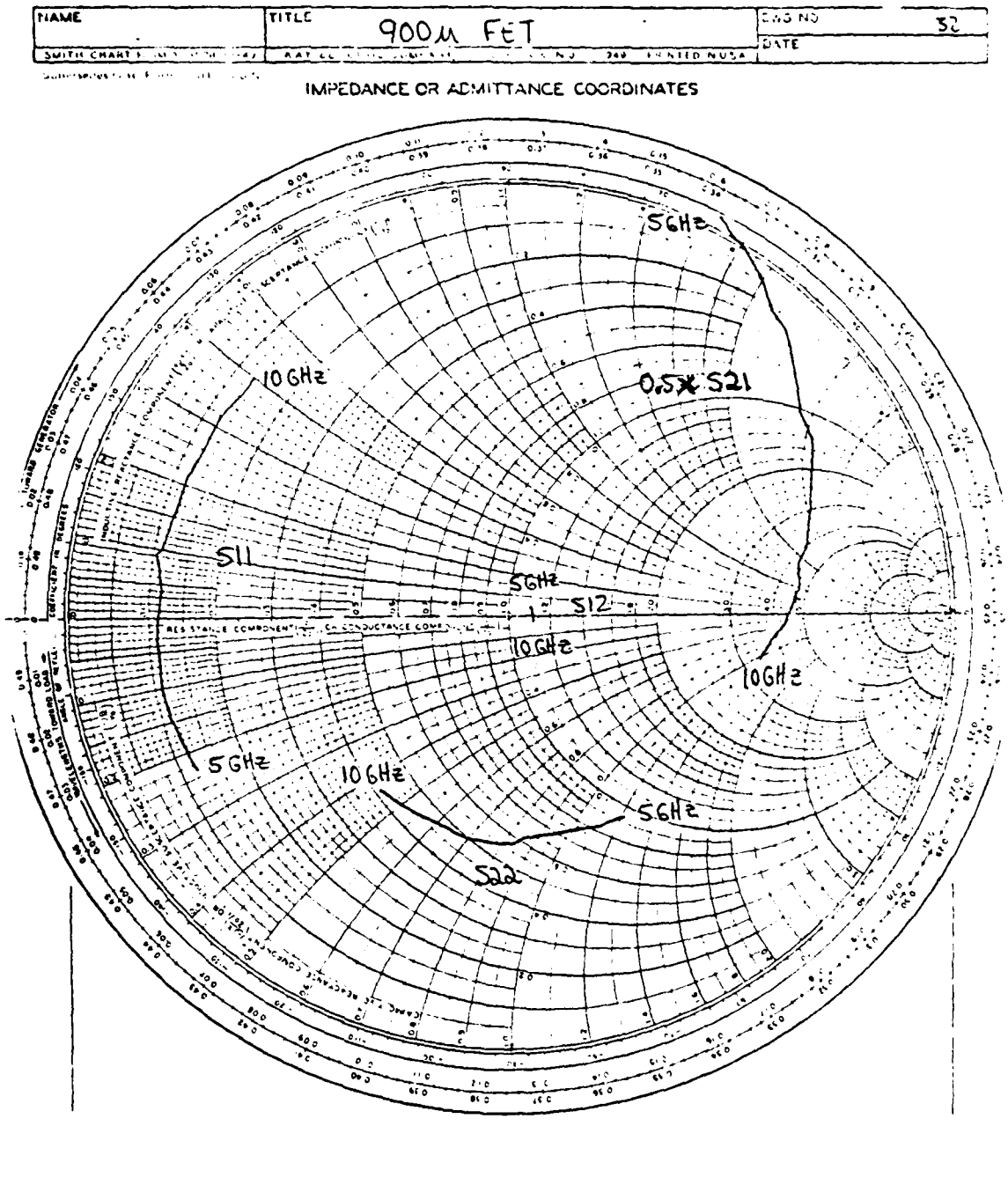
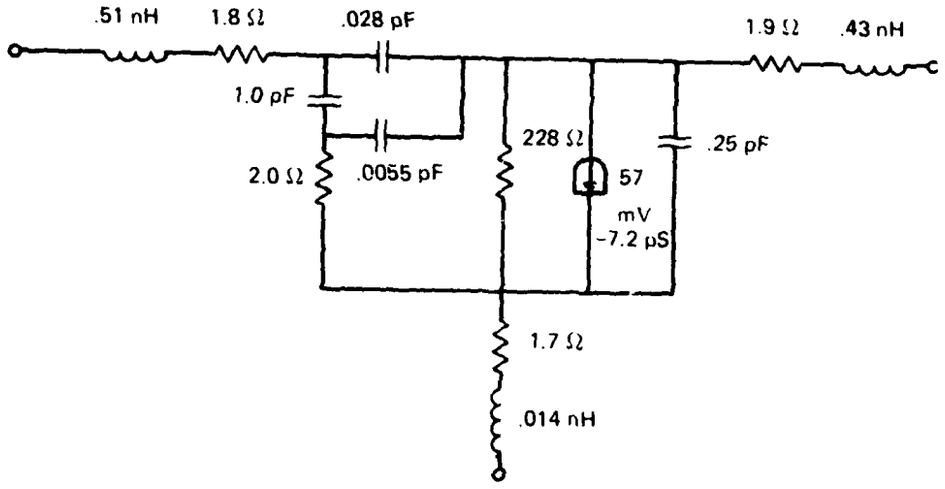
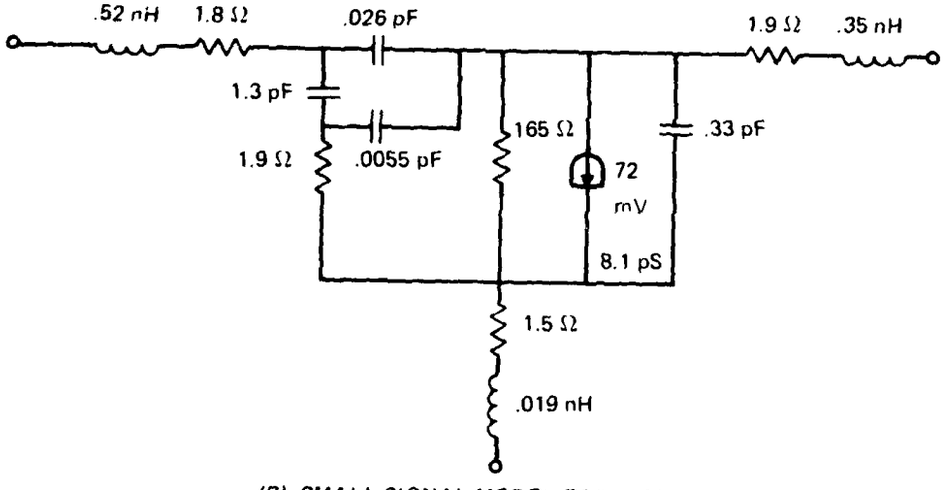


Figure 3-1. Typical S-Parameters of Westinghouse 900 μ FETs



(A) SMALL SIGNAL MODEL FOR 900 μ FET



(B) SMALL SIGNAL MODEL FOR 1200 μ FET

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Figure 3-2a&b. Small Signal Models

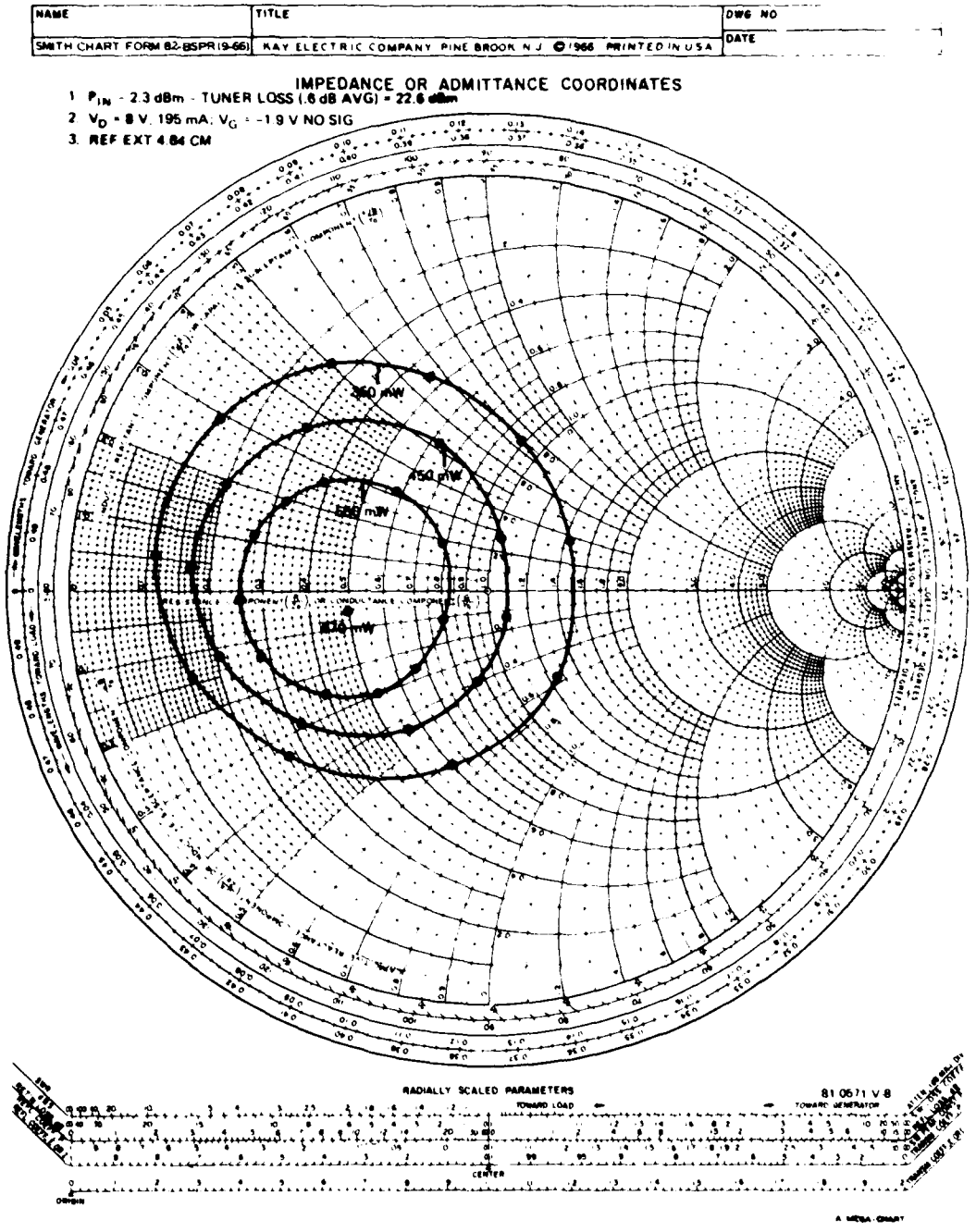


Figure 3-3. Typical Load Pull Data

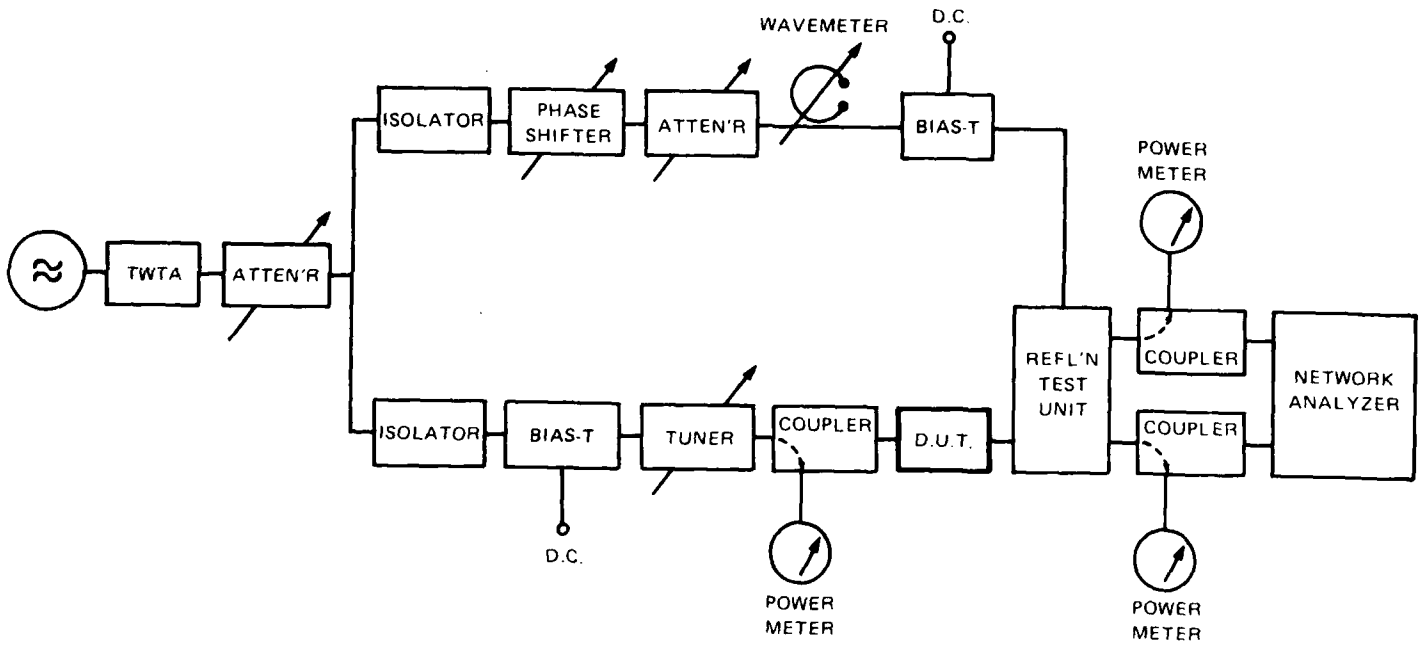


Figure 3-4. Load Pull Schematic

input signal to the FET and then feeds it into the FET output through an attenuator and phase shifter as shown in the figure. The amplitude and phase of the reflected signal can thus be controlled to present any desired impedance to the FET. A network analyzer, in conjunction with two power meters, is used to sample both incident and reflected waves at the output of the FET and display both effective load impedance and net output power, the latter obtained by taking the difference between the incident and reflected power meter readings.

A dedicated test system of this type was set up during this reporting period.

Initially, it was necessary to temporarily use a number of X-band waveguide components in the system, hence the lower frequency limit of the measurements was restricted to $\approx$ 7.5 GHz. Components to assemble a completely coaxial system to operate down to 5 GHz (and lower if desired). These components were received and integrated into the system in time for the measurements for the Mark V designs discussed in section 3.4.

The load pull information along with the measured small signal S-parameters, was the basis for the wideband amplifier design technique discussed in the next section.

3.3 MULTISTAGE WIDE-BAND AMPLIFIER DESIGN TECHNIQUES

The first two-stage amplifier ("Mark 1") was designed by reducing R_D in the small signal model to $R_D/2$ and then designing the input, interstage, and output matching circuits using the network synthesis program, AMPSYN. In this approach the output circuit was essentially matched, with all gain compensation (12 dB) provided by the interstage and input networks.

During the time period when this amplifier was being fabricated, however, extensive load pull measurements were begun on our FETs. These measurements showed that the FETs driven well into compression, which is necessary to achieve good output power and efficiency, the optimum load impedance was much lower than had been previously assumed, making the aforementioned design approach invalid.

During further study of the load pull curves, an amplifier design procedure was evolved which has been used for all subsequent two stage amplifier designs. This design procedure can be summarized as outlined below[1]:

1. For constant power input, load pull contours are generated at 5, 6, 7, 8, 9, and 10 GHz at various output power levels as shown in figures 3-5 through 3-10.

2. From this data, a composite set of contours is assembled representing constant power output (and gain) at each frequency. This is shown in figure 3-11.

3. The output circuit (or interstage circuit in the case of the first stage) is designed to present an impedance locus which crosses these constant power contours in a manner to provide constant power at each frequency.

Thus, the output circuit provides the optimum load impedance at the highest frequency of interest while selectively "de-optimizing" the load impedance at lower frequencies to provide constant power (and gain). This procedure effectively shifts most of the burden of gain equalization to the output and interstage circuits thus simplifying the input circuit design. It also facilitates the achievement of a better input impedance match. Typical impedance/load pull loci, illustrating this technique, for the output circuit and the interstage circuit for the most recent amplifier (Mark V) design are shown in figures 3-12 and 3-13. As mentioned earlier, this design procedure has been used on all two-stage designs starting with the "Mark II" amplifier.

3.4 SINGLE STAGE OCTAVE AMPLIFIER DESIGN AND RESULTS

Prior to the start of the development of the two-stage octave amplifiers, a single-stage 900μ FET octave amplifier was designed, fabricated, and tested. The amplifier, shown in figure 3-14 (a) and schematically in figure 3-14(b) was essentially a test vehicle

[1] J.E. Degenford, R.G. Freitag, D.C. Boire, M. Cohn, "Design Considerations for Wideband Monolithic Power Amplifier," 1980 GaAs IC Symposium Digest, p. 22, Nov. 1980.

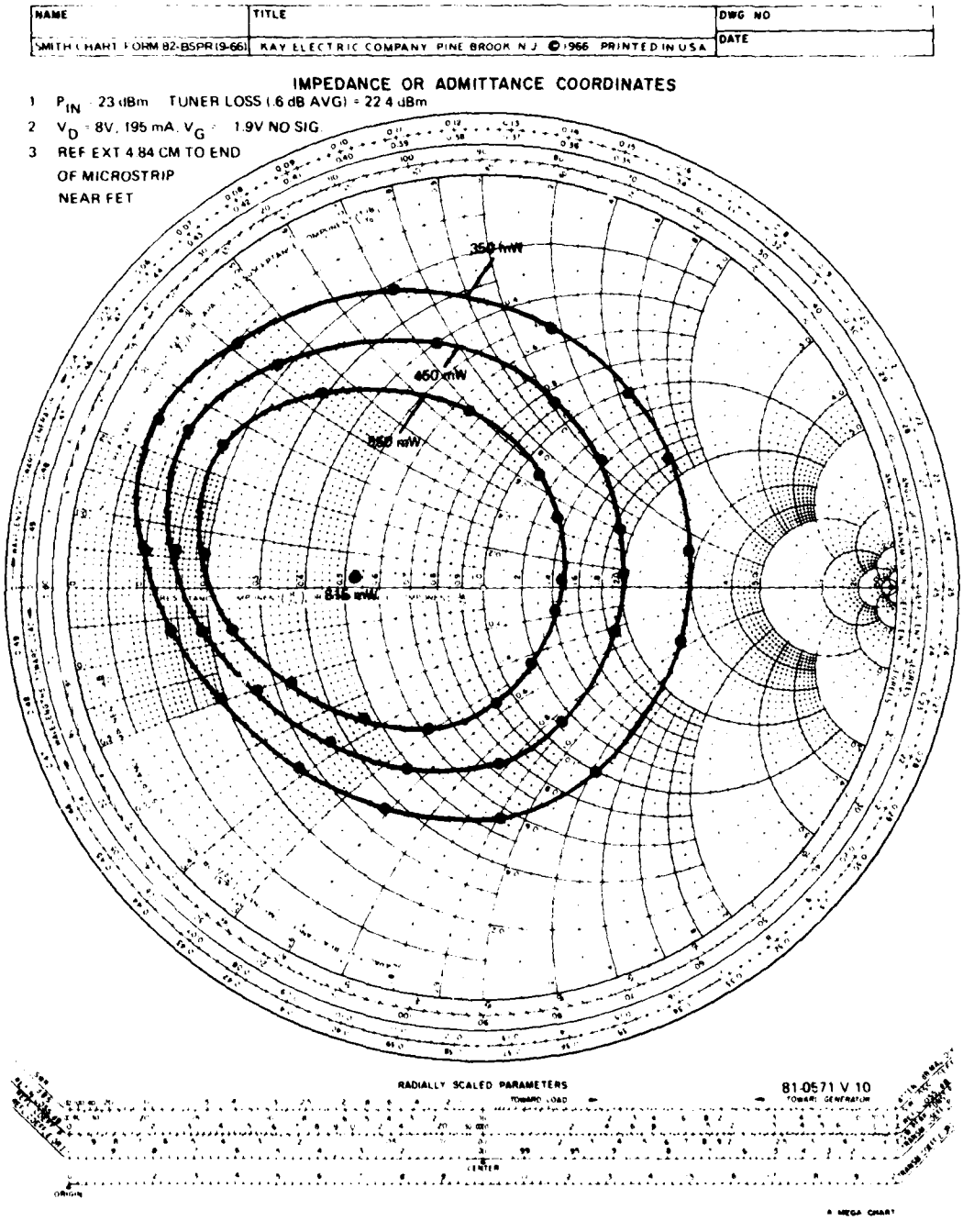


Figure 3-5. Load Pull Contours at 5 GHz

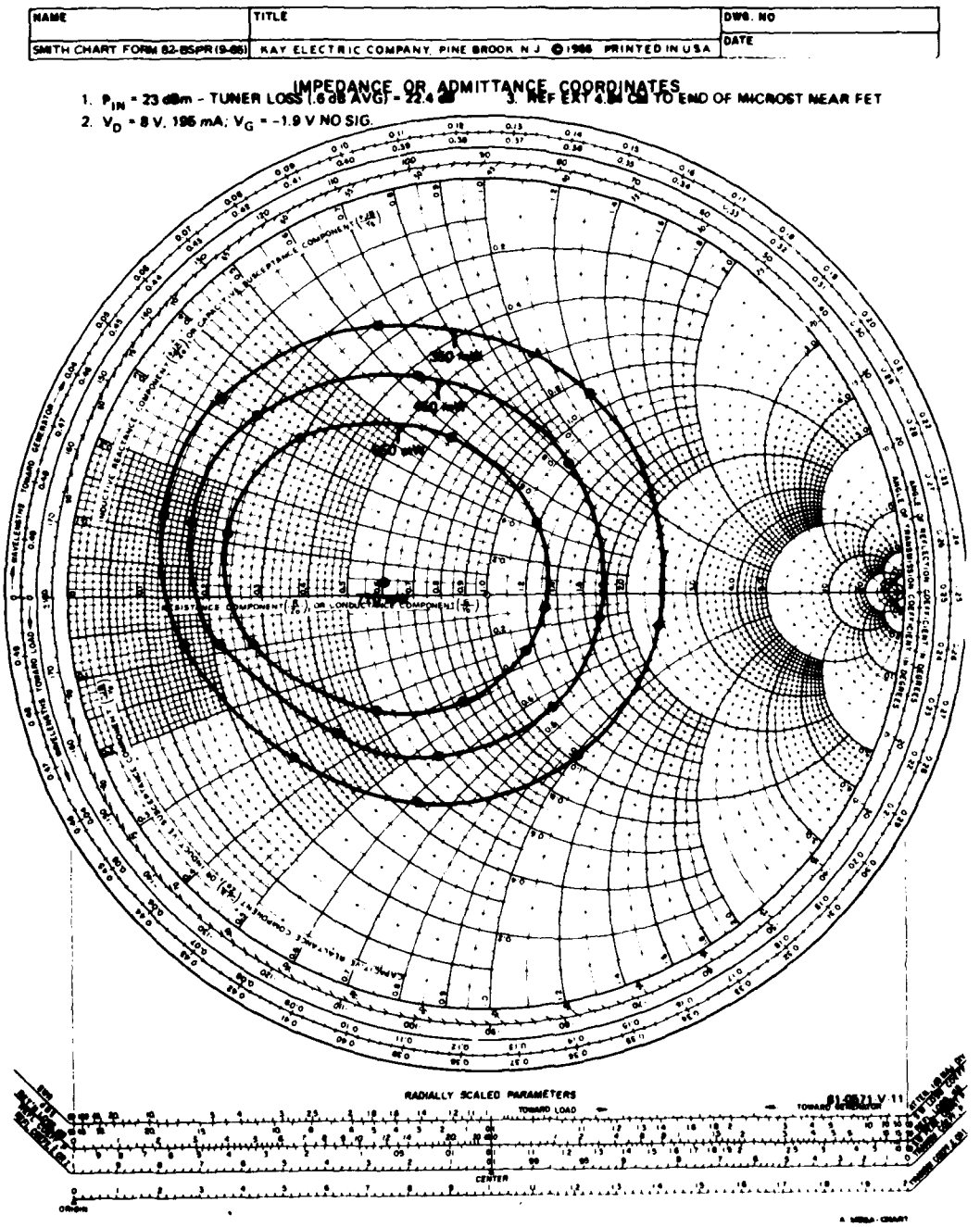


Figure 3-6. Load Pull Contours at 6 GHz

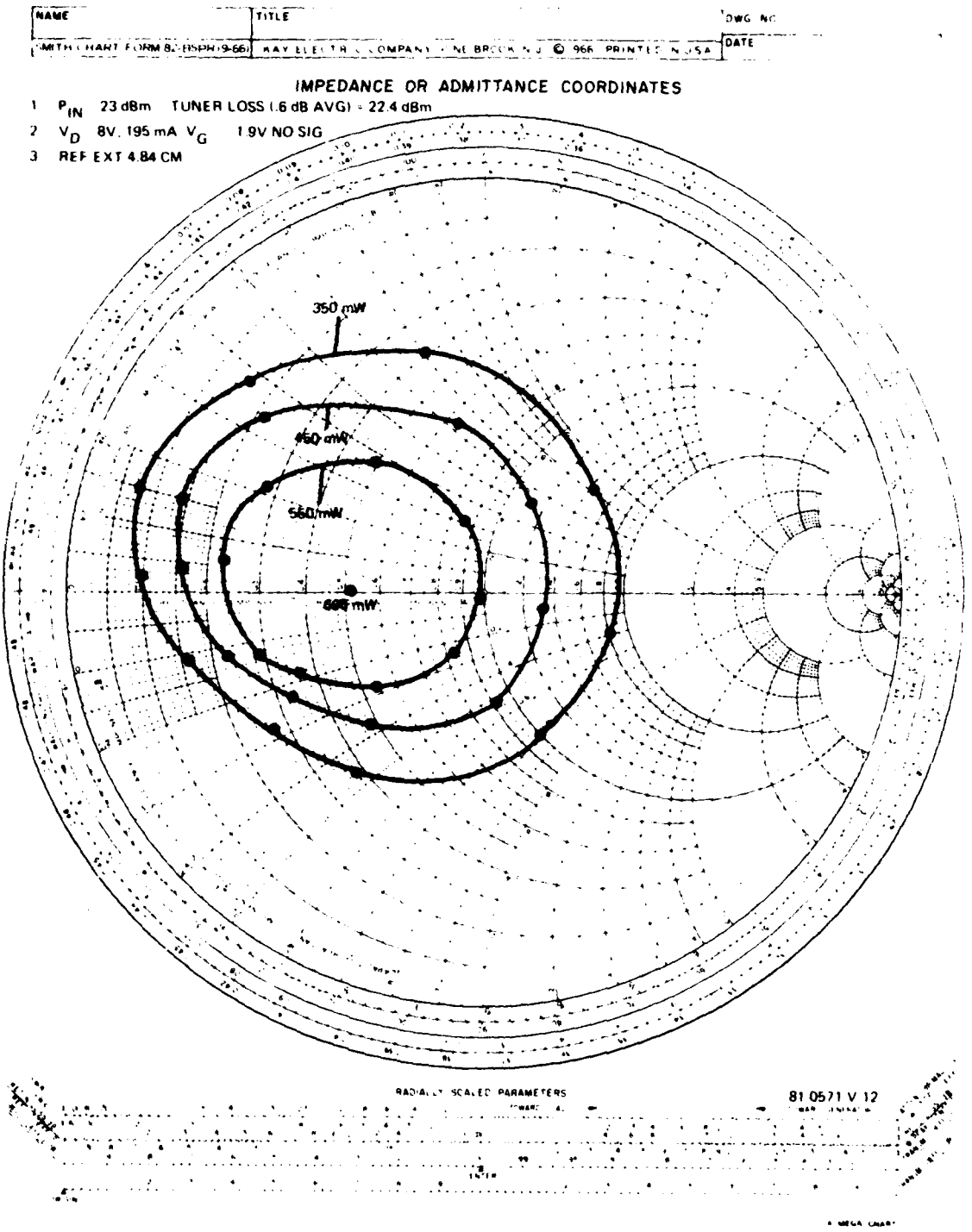


Figure 3-7. Load Pull Contours at 7 GHz

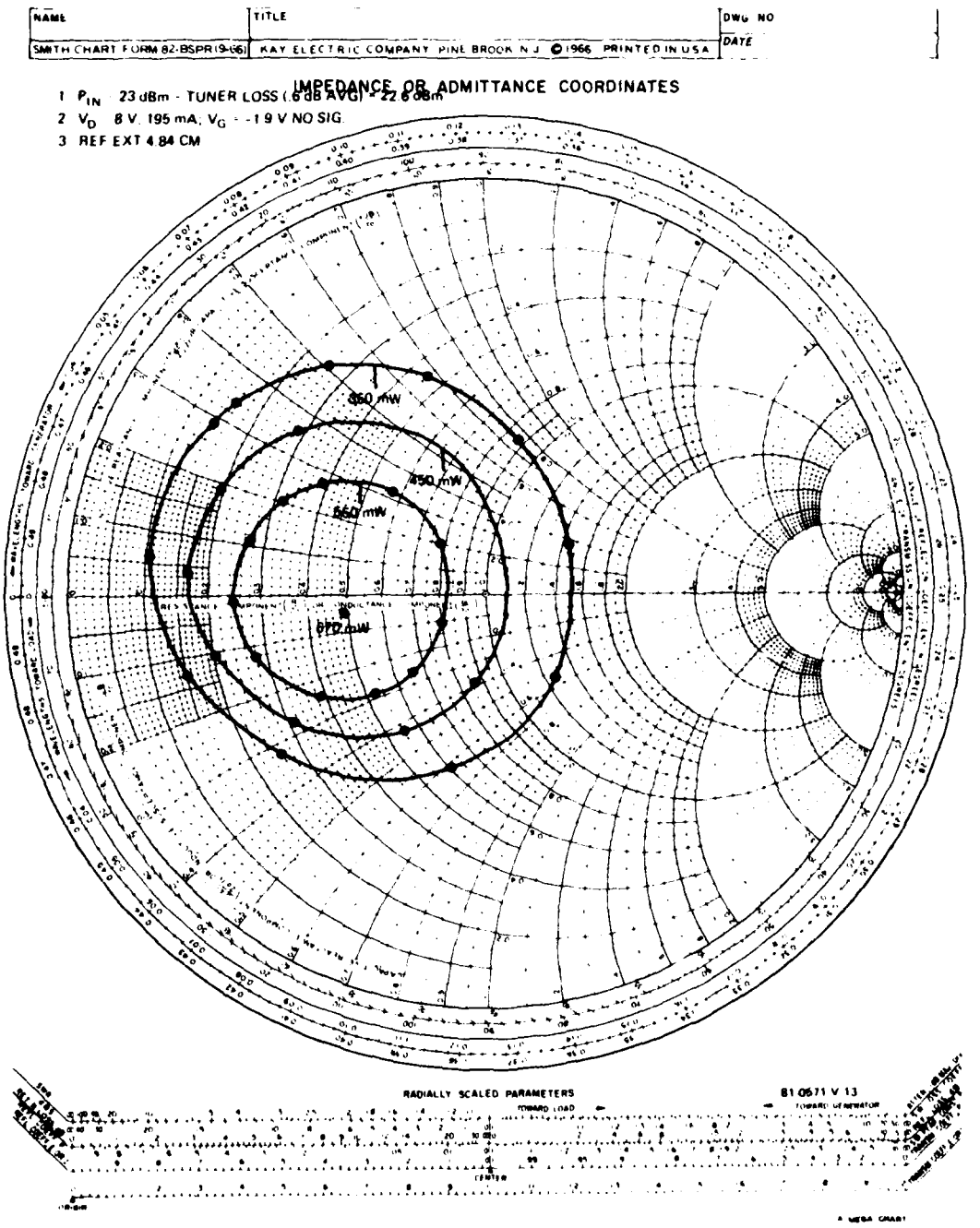


Figure 3-8. Load Pull Contours at 8 GHz

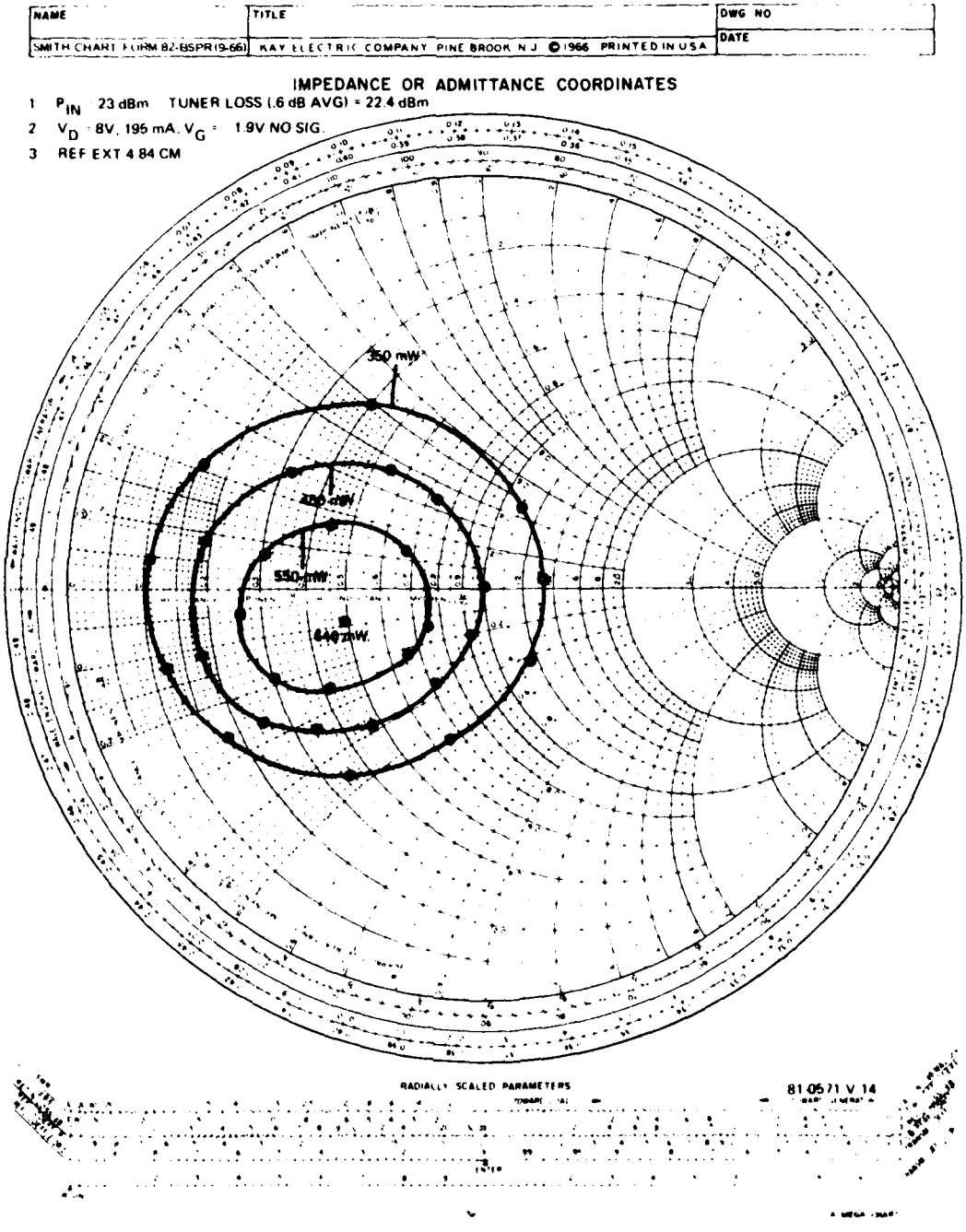


Figure 3-9. Load Pull Contours at 9 GHz

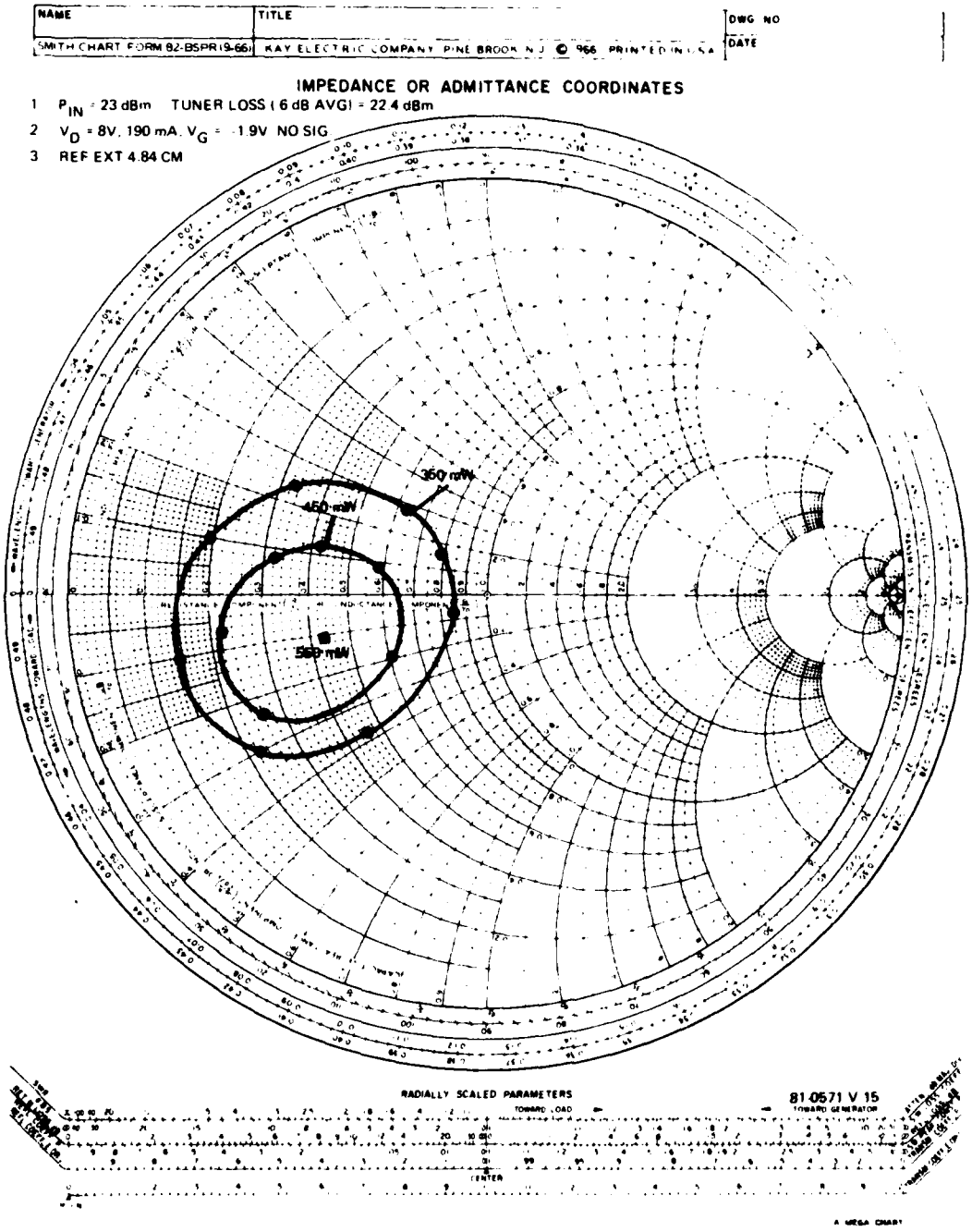


Figure 3-10. Load Pull Contours at 10 GHz

NAME	TITLE	DWG NO
SMITH CHART FORM ZY-01-N	ANALOG INSTRUMENTS COMPANY NEW PROVIDENCE N J 07974	DATE

NORMALIZED IMPEDANCE AND ADMITTANCE COORDINATES

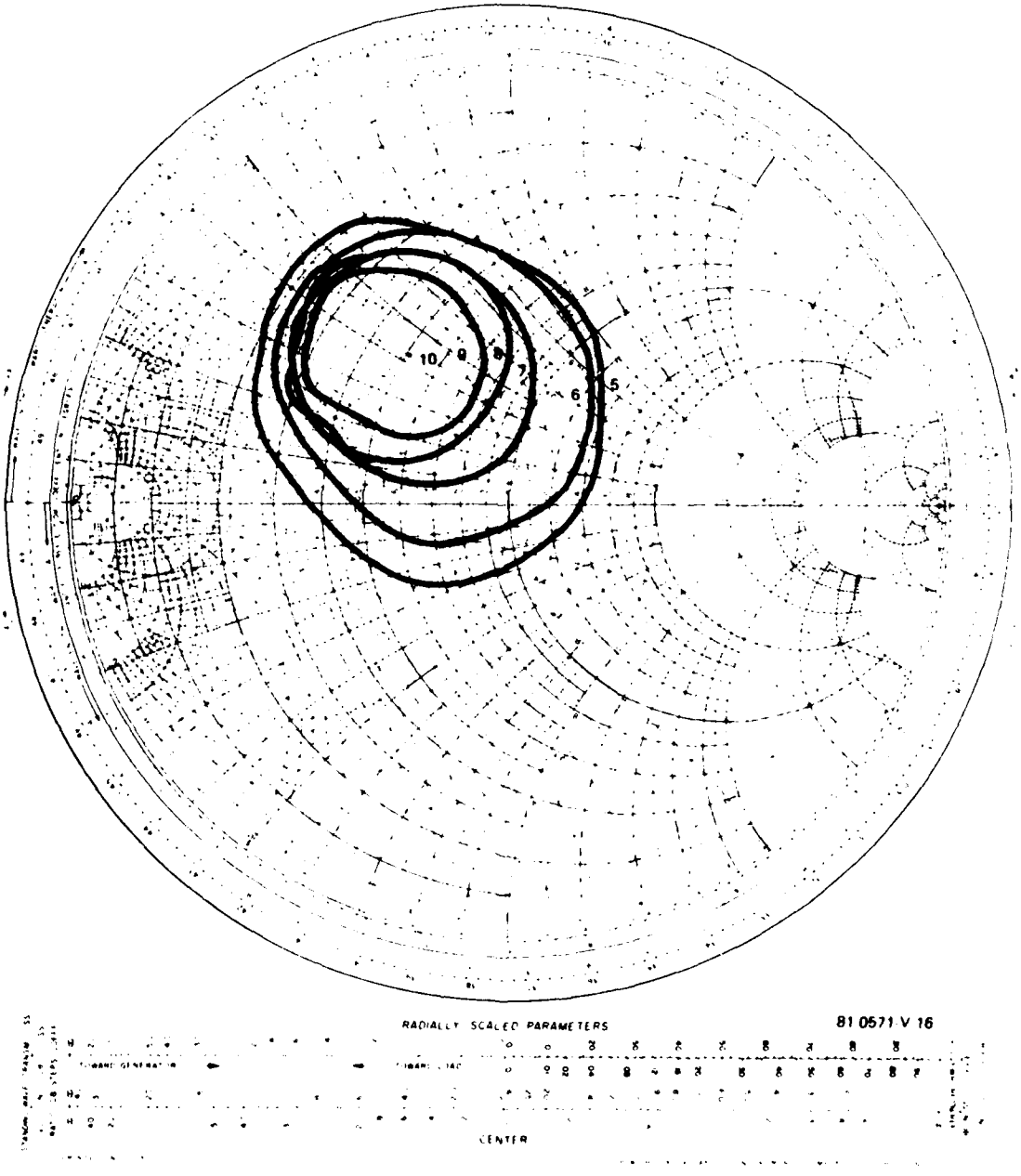


Figure 3-11. Composite Load Pull Contours of Constant Output Power and Gain for 1200 μ FET

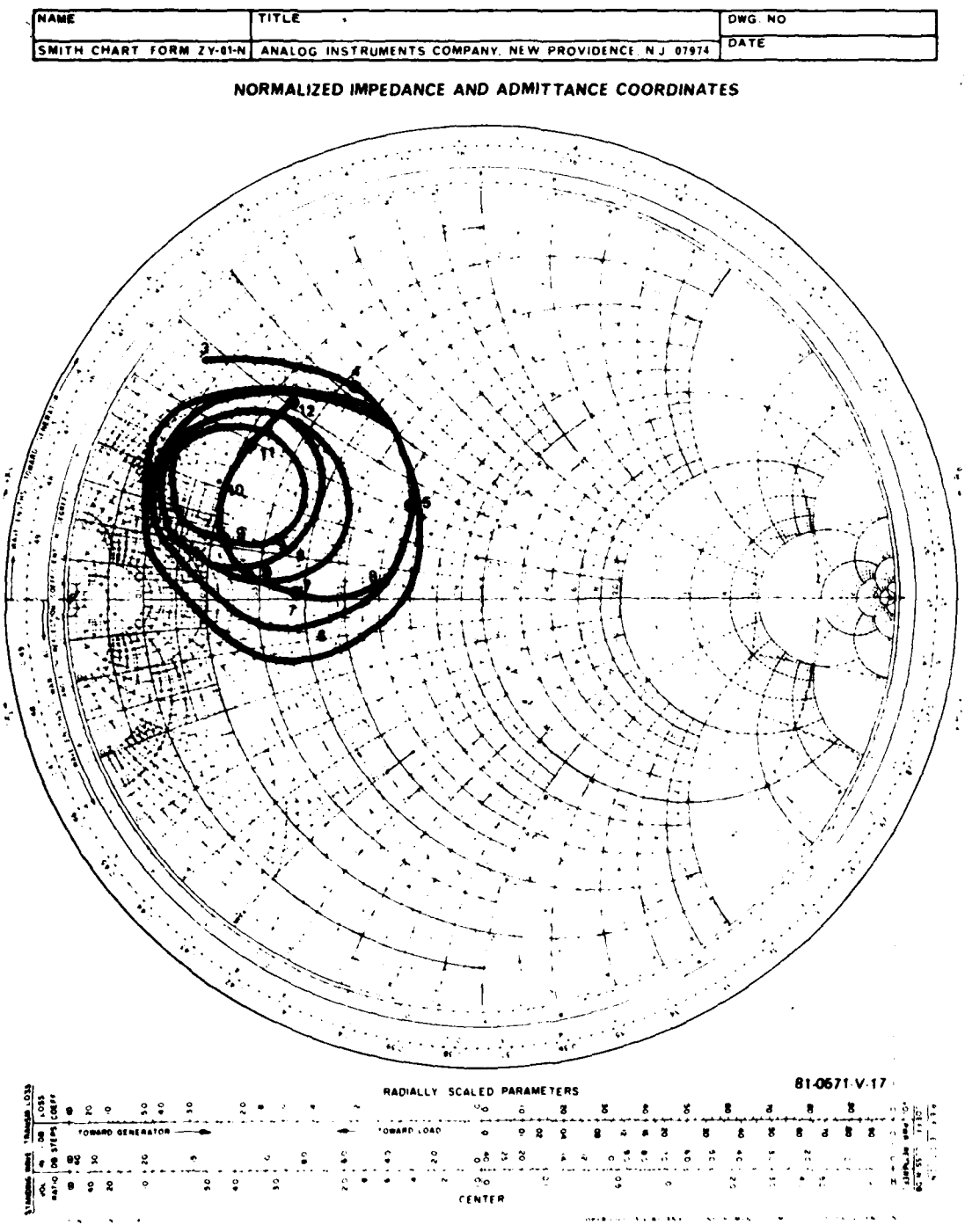


Figure 3-12. Impedance Locus for Mark V Output Circuit Overlayed on Load Pull Contours

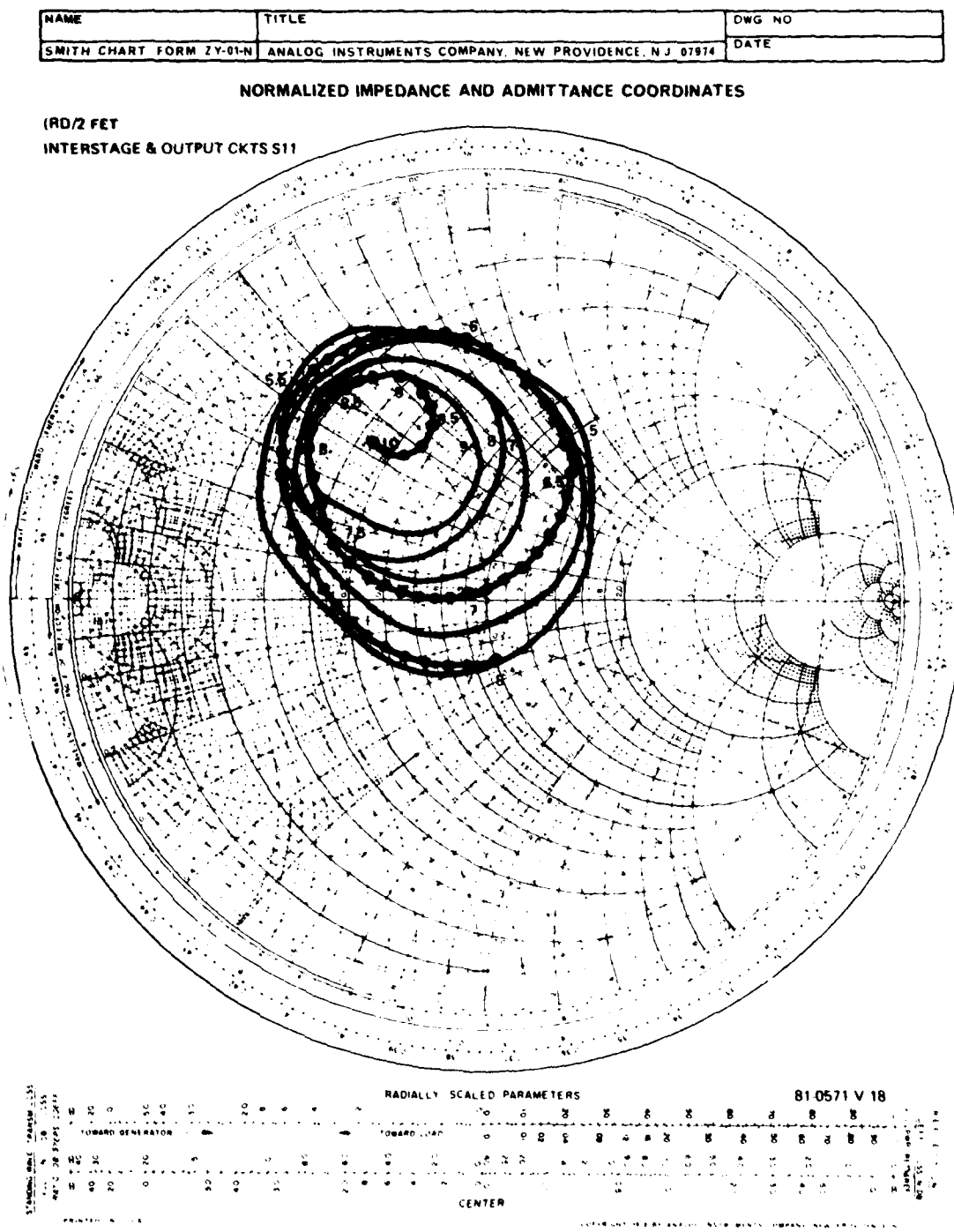
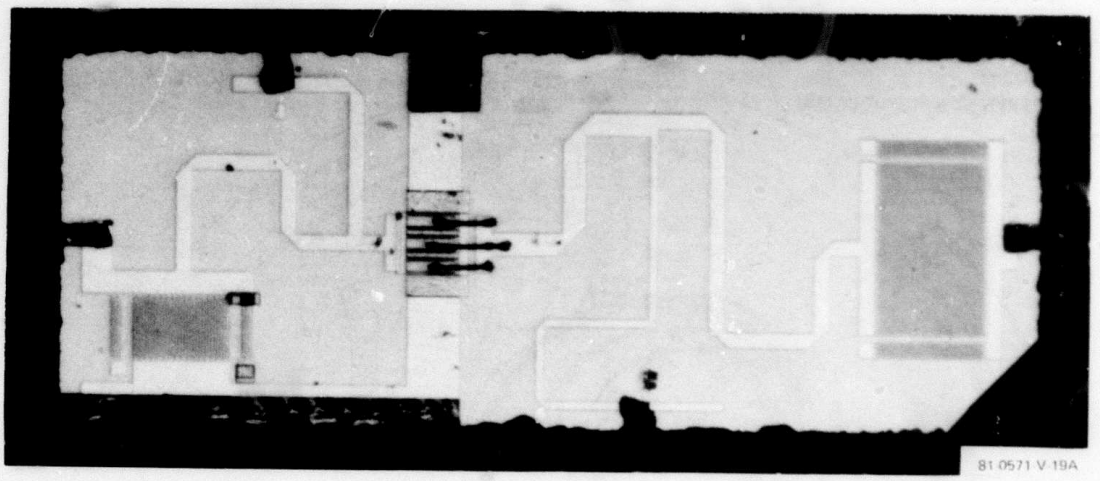
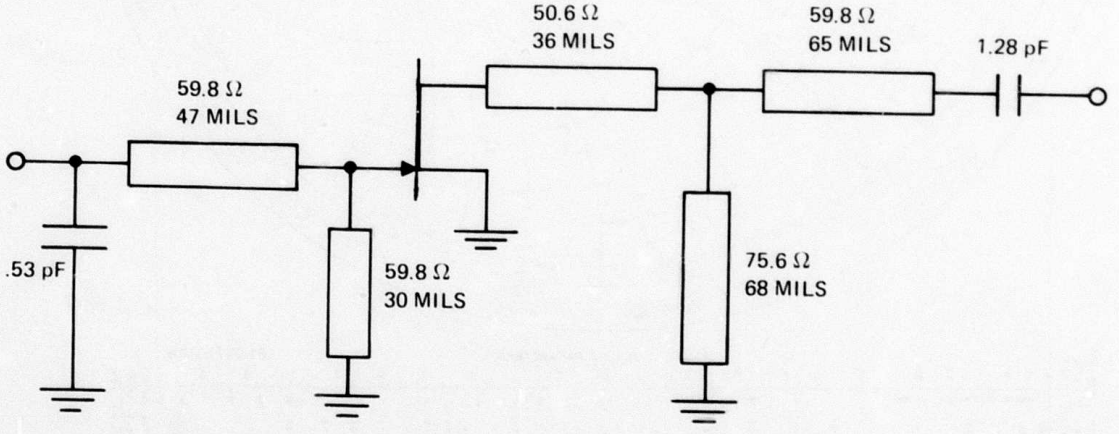


Figure 3-13. Impedance Locus for Mark V Interstage Circuit Overlayed on Load Pull Contours



(a) Amplifier Chip



1(B) AMPLIFIER SCHEMATIC

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Figure 3-14. Single-Stage Octave Band Amplifier

for verifying broadband circuit designs. In addition, extensive on-chip circuit trimming experiments were conducted to verify the predictability and practicality of trimming and to improve the amplifier performance. Trimming is very useful during development since it can significantly speed up development time. A typical amplifier design cycle, from initial inception through mask making, fabrication, and testing takes six to eight weeks. Since the FETs may be evolving and improving during this time, it is important to have flexibility to trim the amplifier to compensate for minor FET changes, otherwise an entire run might be lost due to FET variations. The information obtained by trimming then provides guidance for the next amplifier design.

Untrimmed power results on one of the best amplifiers (IC10C2) from run IC10 are shown in figure 3-15. Note that this amplifier produced 100 mW output from 5 to 9.9 GHz with 5 dB gain, 200 mW from 5.0 to 9.0 GHz with 5 dB gain, 300 mW from 5 to 8.4 GHz with 4.5 dB gain, and 400 mW from 5 to 7.5 GHz with 4.0 dB gain. While this amplifier exhibited basically a flat small signal response as shown in figure 3-16, the more typical amplifier from this run exhibited a high frequency rolloff even under small signal conditions as shown in figure 3-16 for amplifiers IC10C8 and IC10C6. In an effort to determine the cause of this rolloff, a careful study of the amplifier layout as compared to the original circuit design was made which revealed the following items:

- A short 0.006" transmission line had been added during mask layout at the gate to move the shunt inductor in the gate away from the source metallization.
- Because the chip was wider than the discrete chip on which the original measurements had been made, the source metallization, and hence, source inductance was larger than designed.
- Circuit metal thickness of 1.3 microns was less than the optimum 2-3 microns for minimum loss.

The cumulative effect of these changes as shown in figure 3-17 by the dotted curve is a significant gain loss at the top end of the band. This predicted curve is replotted on figure 3-16 (solid curve) and the trends agree well with the two amplifier results,

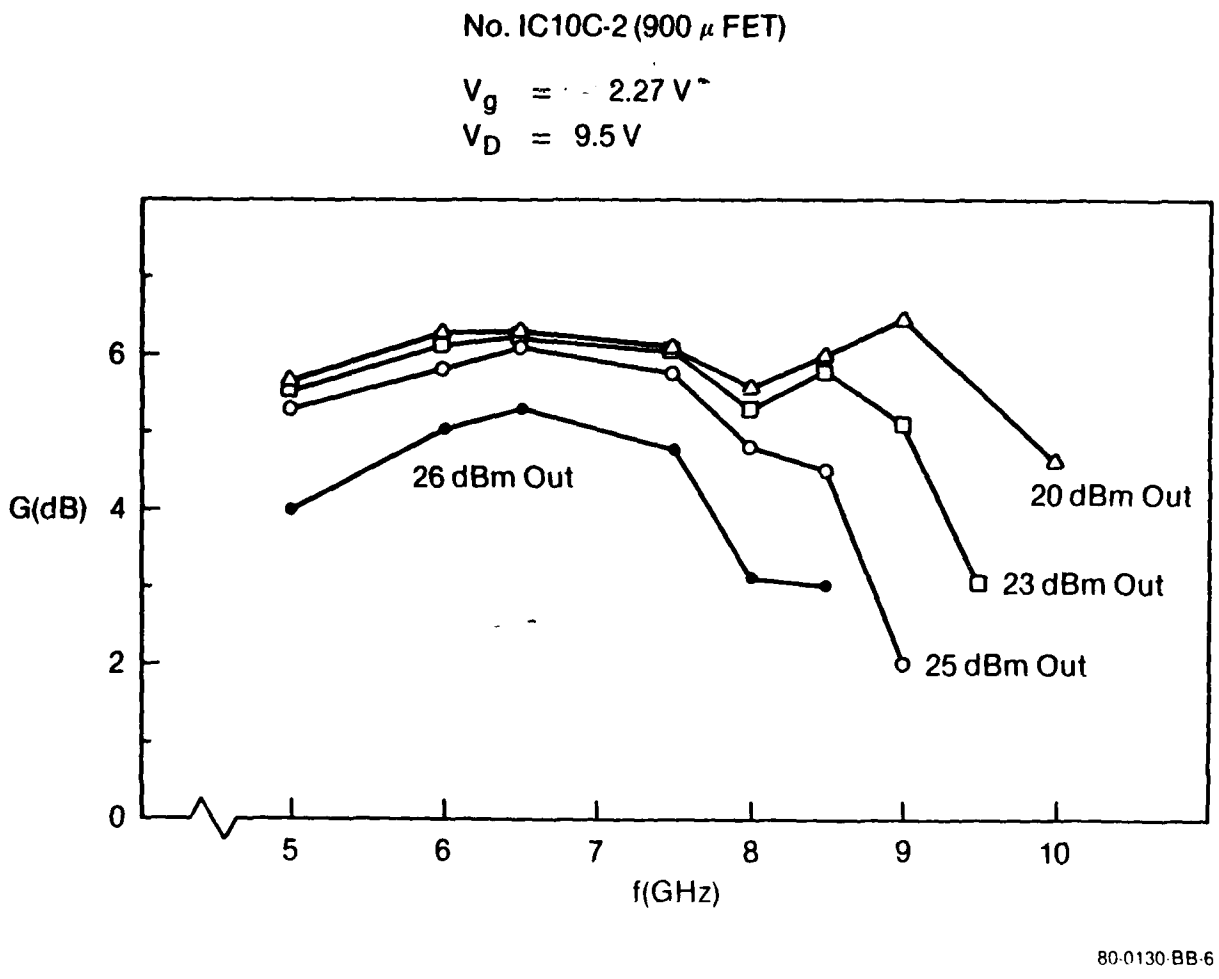

Figure 3-15. Single-Stage Octave Band Amplifier Power Results

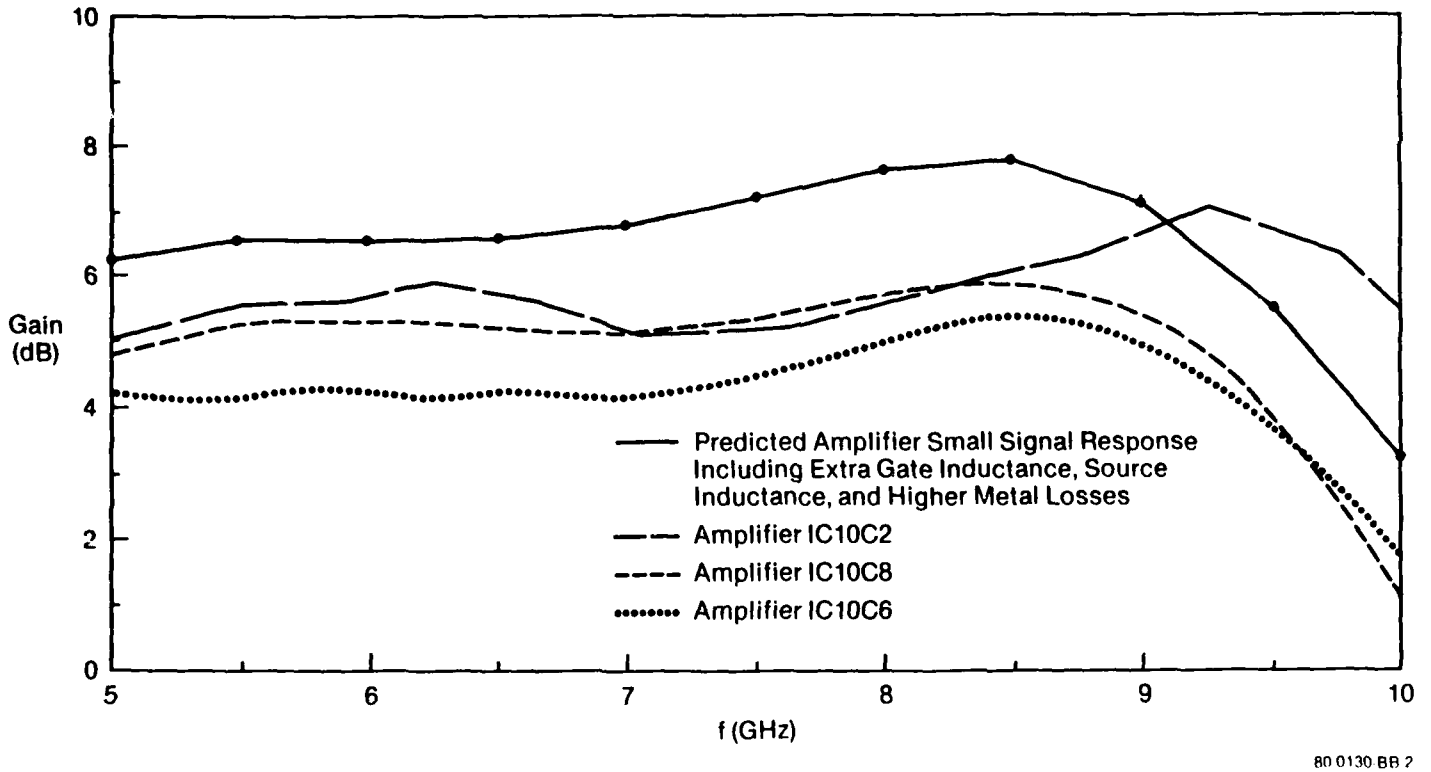

Figure 3-16. Comparison Between Measured and Predicted Amplifier Gains

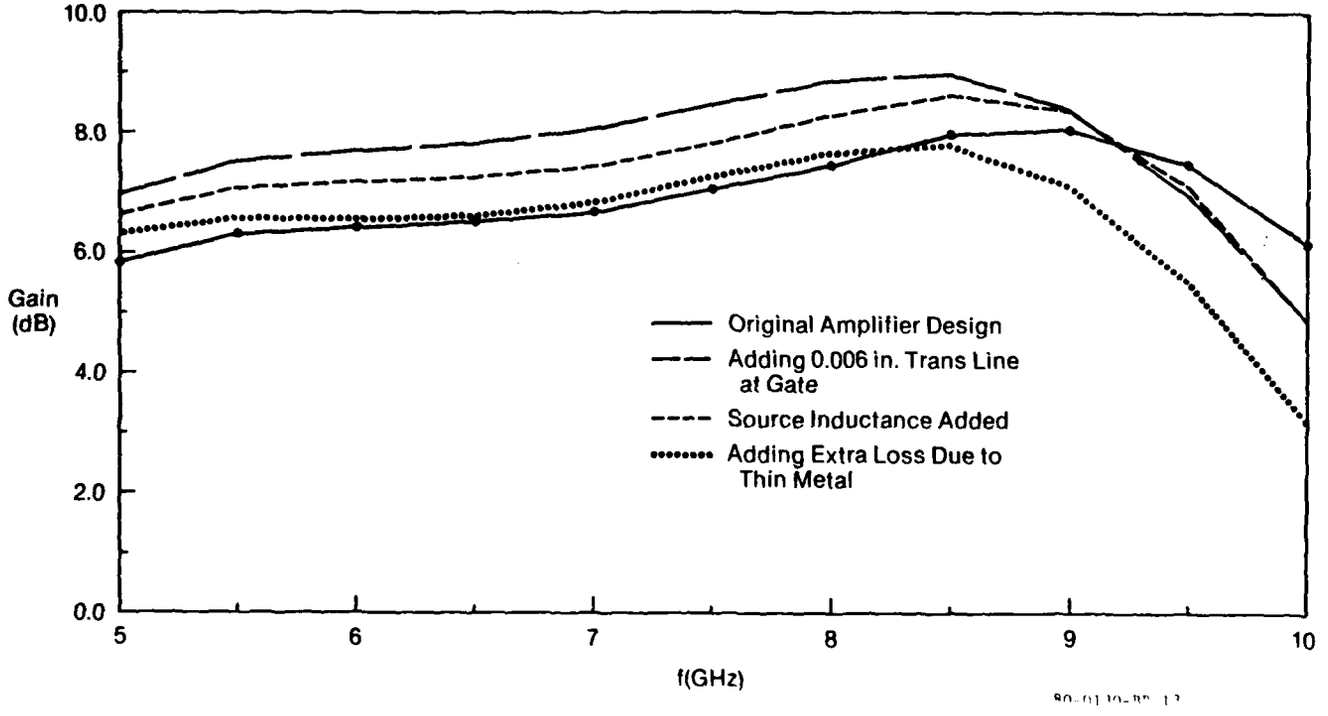

Figure 3-17. Predicted Small Signal Gain of Single-Stage Amplifier

IC10C8 and IC10C6, although the measured amplifier gains are consistently slightly lower than the predicted value.

In an attempt to improve the frequency response at the upper band edge a study was made on the effects of trimming these amplifiers. Since the gate-source input circuit was found to have more inductance than originally planned, the effect of decreasing the input series inductance was studied. This inductance is the inverted U-shaped piece of transmission line connecting the input shunt capacitor to the gate of the FET in figure 3-14. Figure 3-18 shows the effect of shortening this inductor by 1) bonding a ribbon halfway across the "U", and 2) by bonding 2 ribbons to effectively bypass the "U" of the transmission line. As can be seen, the gain response is optimized for case 1 above. Note that, compared to the untuned response, the tuned response is improved significantly at the top end of the band, degraded slightly in the middle of the band, and improved slightly at the lower end of the band. Measured results of tuning an amplifier in this fashion are shown in figure 3-19, and show excellent agreement with the predicted response.

It should be noted that the preceding trim experiments were carried out under small signal conditions for convenience in making rapid swept measurements. An experiment to improve the output power at the upper edge of the band was also performed and was very successful. By shortening the two output inductors on the chip, 400 mW output power was achieved across the bandwidth with 3 dB minimum associated gain. This tuning was not optimum, from the standpoint of both power and gain, nonetheless, it did confirm the trimming procedures under power conditions.

3.5 TWO-STAGE AMPLIFIER DESIGNS AND RESULTS

3.5.1 Introduction

Five two-stage monolithic amplifiers were designed during this reporting period. Each is discussed in more detail in the following sections.

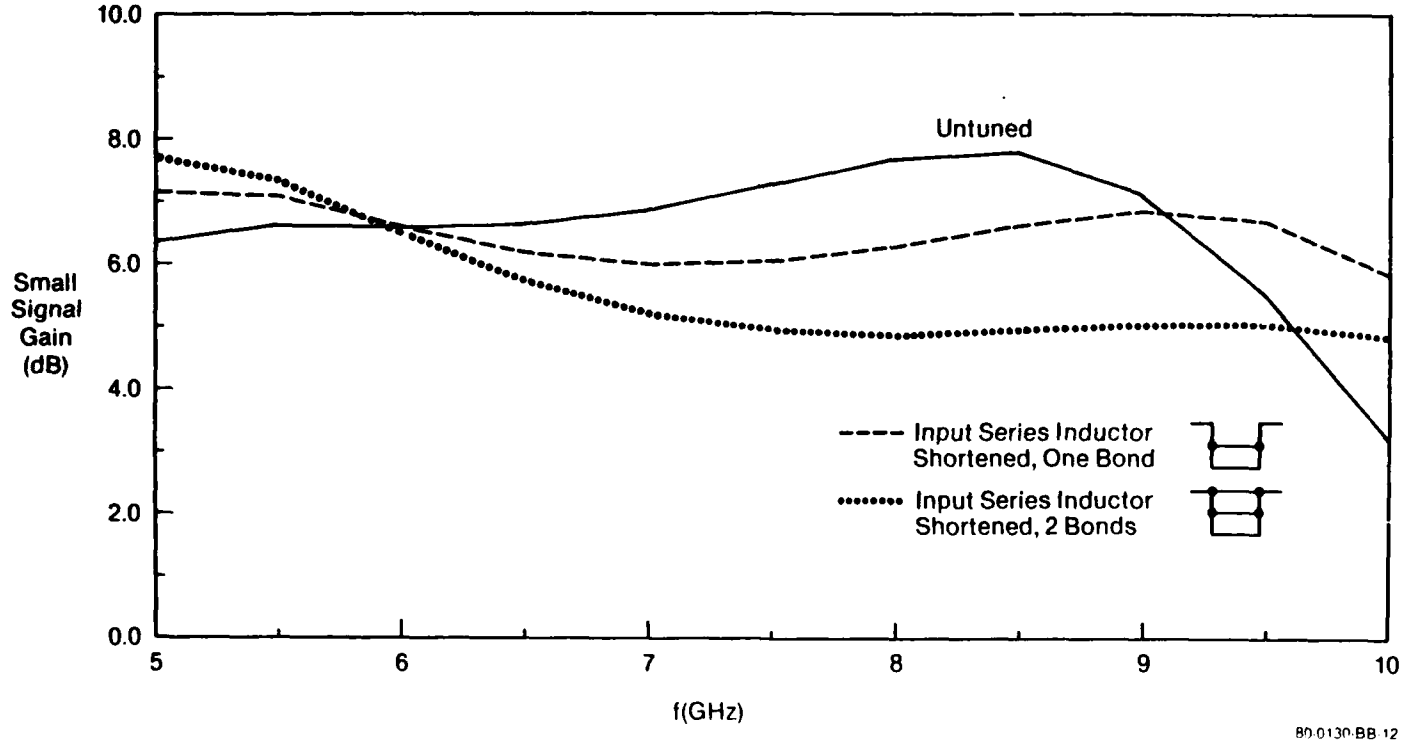

Figure 3-18. Predicted Effects of Trimming on Small Signal Gain of ICIO Amplifiers

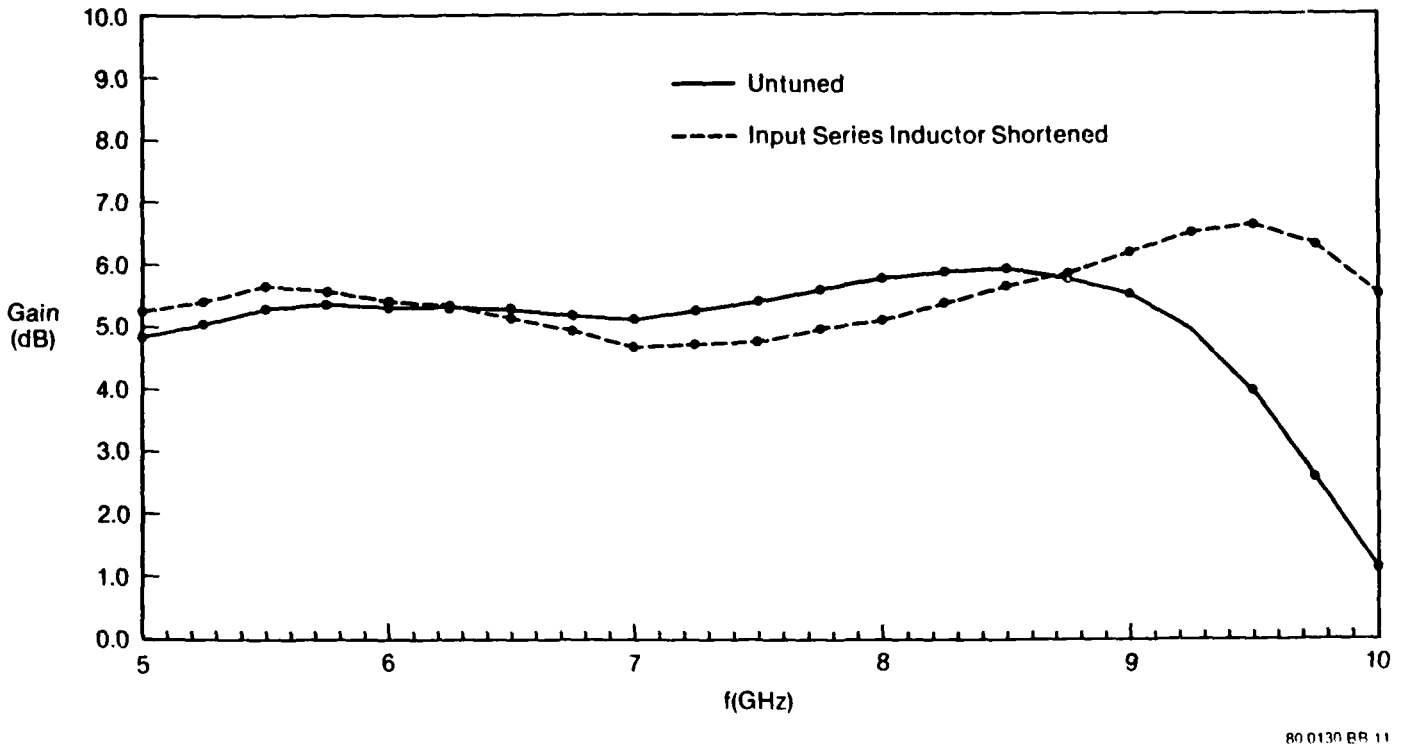

Figure 3-19. Measured Effect of Tuning Input Series Inductance on Gain Response of Single-Stage Amplifier

3.5.2 Mark I Amplifier

The first two-stage amplifier to be fabricated shown in figures 3-20 and 3-21, utilized a 900μ FET in the first stage and a 2400μ FET in the second stage. Large signal FET response was approximated by using the small signal FET model with the drain-source resistance dropped to half its small signal valve. Each matching network included a series capacitor which doubles as a tuning element and a dc block. Biasing was accomplished through shunt inductors connected to large (18pF) off-chip capacitors. These inductors were also used as tuning elements.

This amplifier had interdigital capacitor fingers oriented in two directions and suffered from metal liftoff problems on the capacitor fingers leading to zero yield. Later designs were constrained to have all the fingers oriented in the same direction to eliminate this problem.

3.5.3 Mark II Amplifier

This two-stage amplifier was designed so that each stage was a separate one-stage amplifier with 50Ω terminating impedances as shown in figure 3-22 and 3-23. This temporary design approach permitted dividing the two-stage amplifier chip into two single-stage chips each of which had accessible input and output ports. That facilitated testing of the individual stages for diagnostic purposes. It utilized a 900μ FET in the first stage and a 2400μ FET in the second stage. The impedance of the output matching circuit for each stage was designed to cross the load pull contours to produce constant power and gain at each frequency. The load pull contours were only available, however, over the frequency range of 7 to 10 GHz due to equipment limitations. Load pull contours for the lower portion of the band were extrapolated. The input circuit was designed to match the small signal input impedance of the FETs because this impedance has been shown to be nearly independant of drive level. The resultant S_{11} of the amplifier is shown in figure 3-24.

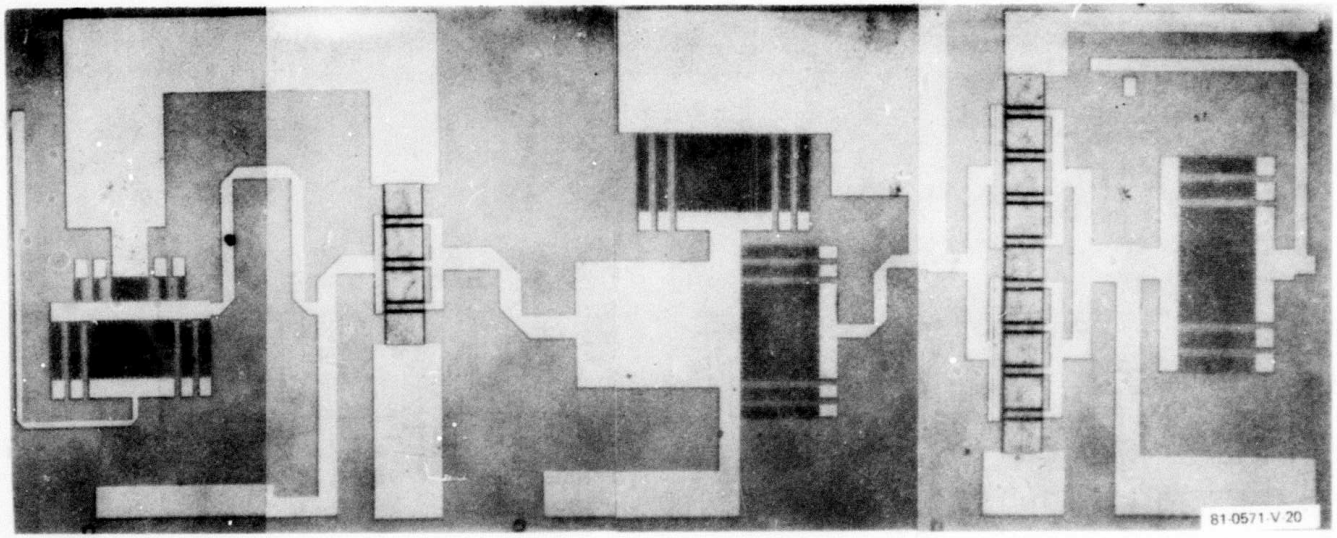

Figure 3-20. Mark I Amplifier

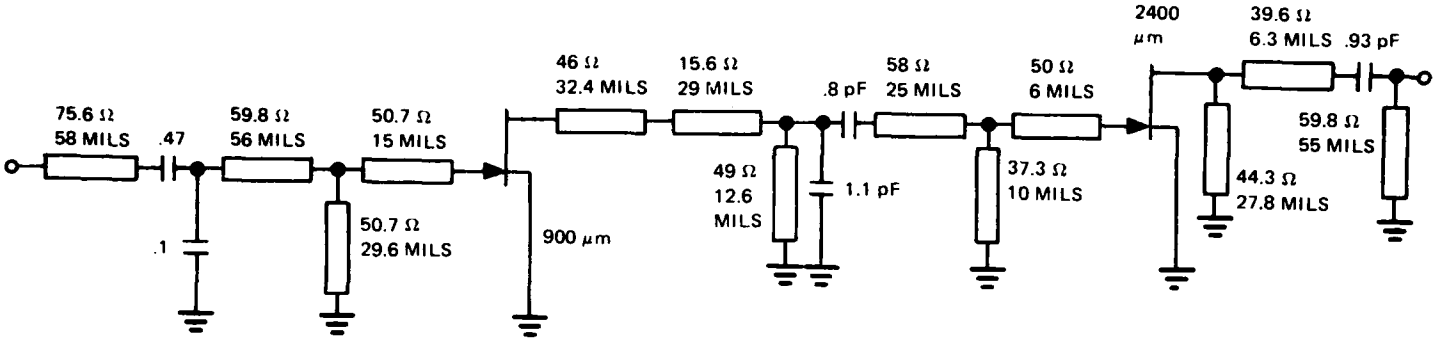

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Figure 3-21. Mark I Amplifier Schematic

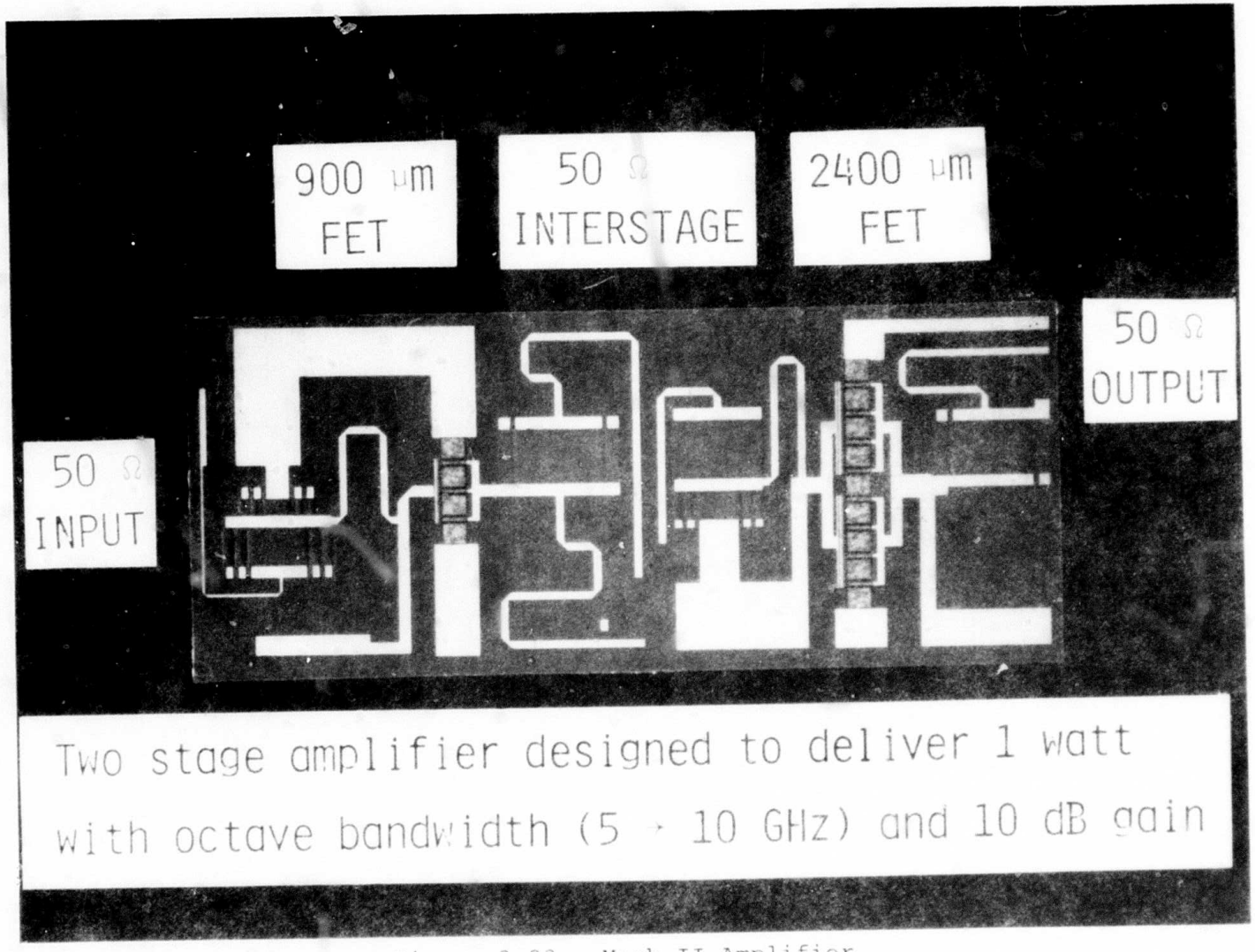


Figure 3-22. Mark II Amplifier

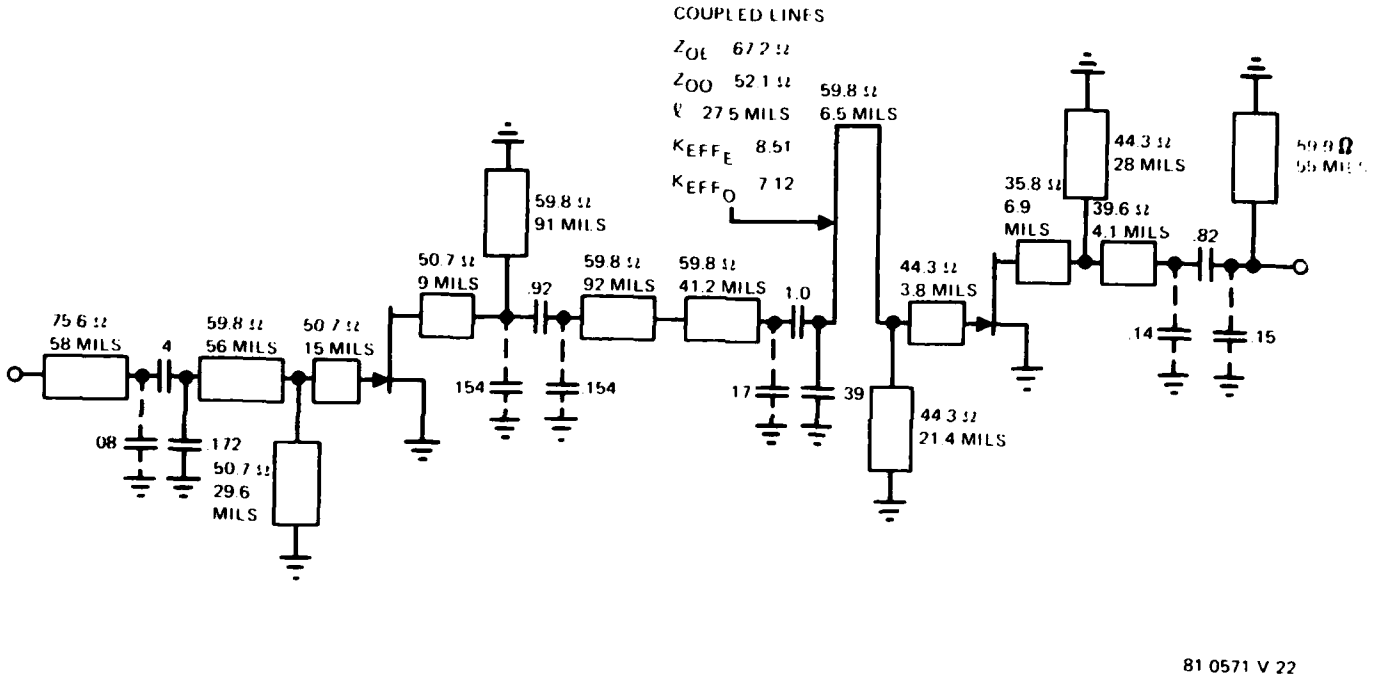


Figure 3-23. Mark II Amplifier Schematic

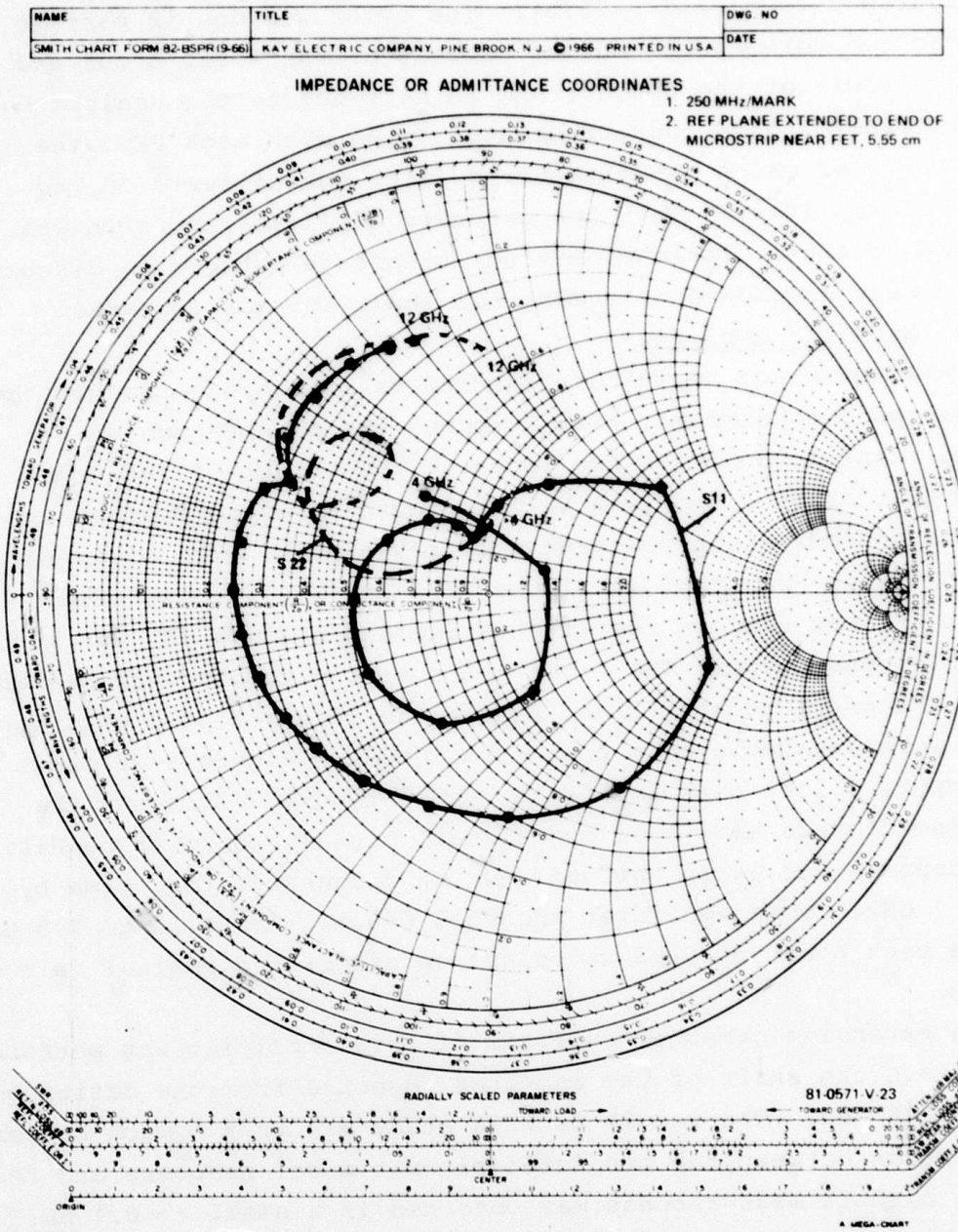


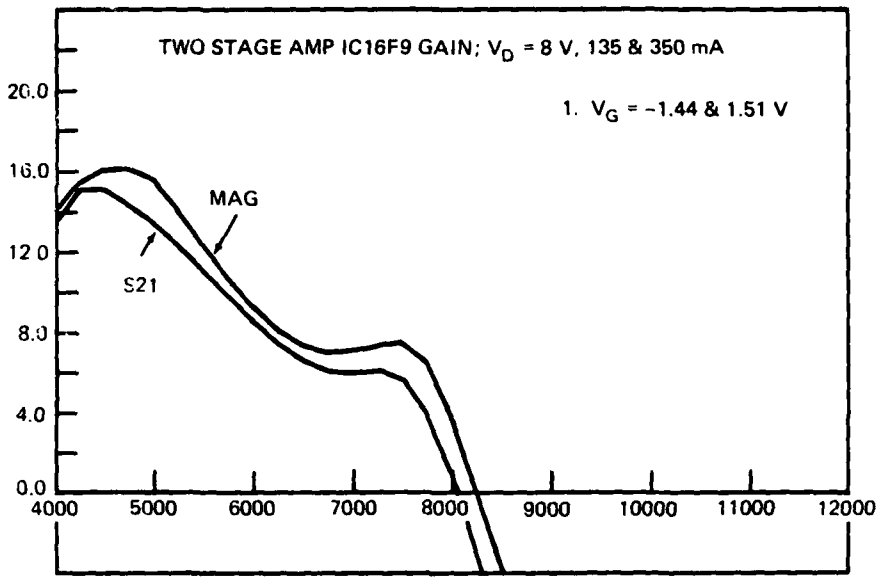
Figure 3-24. Mark II Small Signal S_{11}

The response of this amplifier under small signal and power conditions was shifted down in frequency by about 2 GHz as shown in figures 3-25(a) and 3-25(b). The shift was due in part to interaction between the output circuit of the first stage and the input circuit of the second, and in part due to the neglecting of an "intrinsic" gate inductance associated with each FET, the importance of which was discovered later during tests on the Mark III amplifier. This two separate amplifier approach was not pursued further. Instead, a true interstage network as discussed in the next section on the Mark III amplifier was designed.

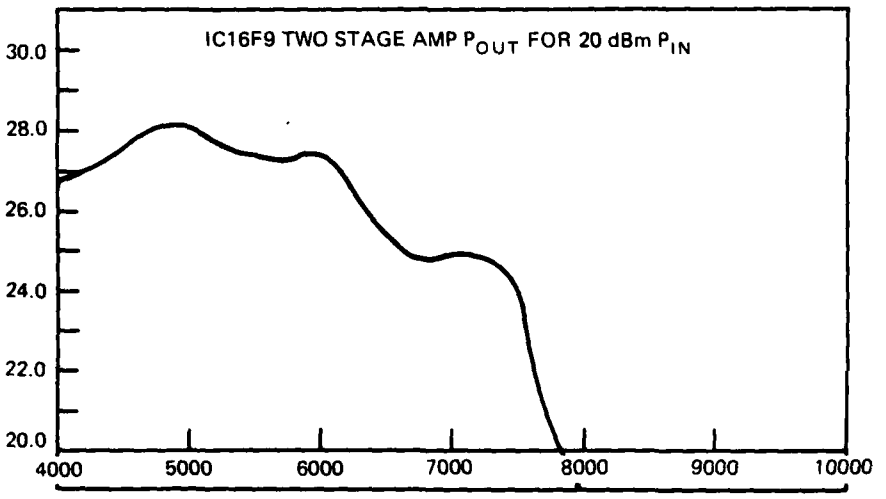
3.5.4 Mark III Amplifier

This two-stage amplifier featured an interstage circuit that was designed to directly transform the input impedance of the second stage to an impedance locus at the output of the first stage that crossed the load pull contours so as to produce constant gain and output power at all frequencies. The amplifier and schematic are shown in figure 3-26 and 3-27, respectively. A 900μ FET was used in the first stage and a 2400μ FET was used in the second stage. The input and output circuits were designed as in the previous amplifier. Again the measured load pull contours were available only from 7 to 10 GHz. Figure 3-28 shows the input, S_{11} of this amplifier, while figure 3-29 shows the response of this amplifier under small signal and power conditions. The response was again shifted down in frequency, this time by about 1 GHz. This amplifier produced 660 mW from 4.25 to 7.5 GHz with a peak power of 0.82 watts and an associated nominal gain of $\simeq$ 7 dB.

An extensive computer analysis of this amplifier was performed to explain the shift of the measured response from the design goal of 5 to 10 GHz. The result of this study was that a much better correlation between the predicted circuit model response and the actual circuit measurements was obtained if a small ($\simeq$ 0.1 nH) series inductance was added to the gate side of the FETs used in the design. The implication of this analysis was that a small



(A) SMALL SIGNAL



(B) LARGE SIGNAL

81-0571-V-24

Figure 3-25. Mark II Amplifier Response Curves

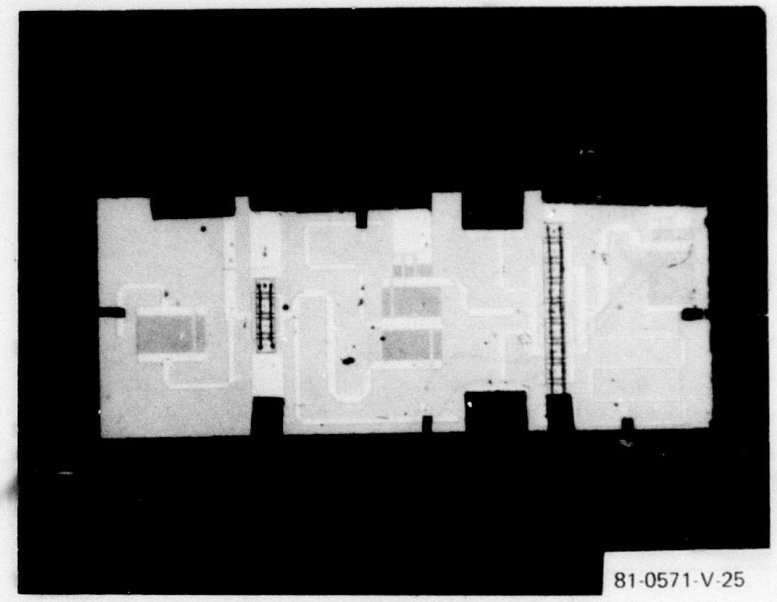


Figure 3-26. Mark III Amplifier

0.1 nH gate inductance should be included in the intrinsic FET model used for amplifier design. This was done in the Mark IV design discussed in the next section with good results.

An attempt was made to trim this amaplifier to increase its high frequency response. By shortening the bias inductor for the 900μ FET, the power output in the 8.5 - 9 GHz range was significantly improved as predicted. Over 900 mW as obtained at 9 GHz with 6.8 dB associated gain.

3.5.5 Mark IV Amplifier

This amplifier shown in figures 3-30 and 3-31 was essentially a second iteration of the Mark III design. The intrinsic FET models used in this design included a small gate inductance as indicated from Mark III analysis in an effort to increase the high frequency response. Circuit vias were employed for improved source grounding (lower inductance) and increased circuit flexibility. Measured load pull design data was available only from 7 to 10 GHz.

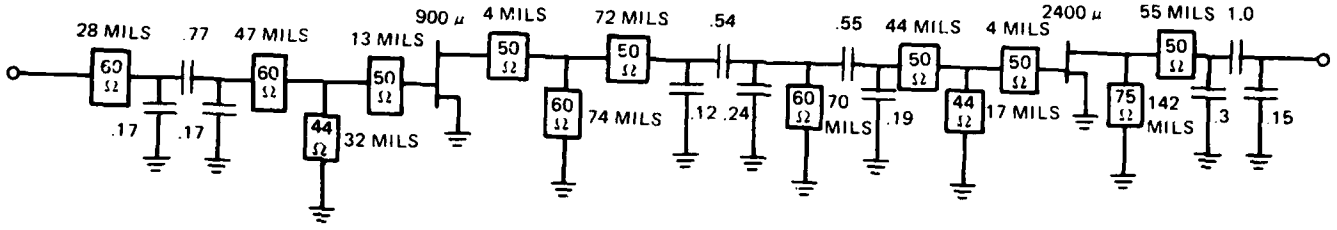


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Figure 3-27. Mark III Amplifier Schematic

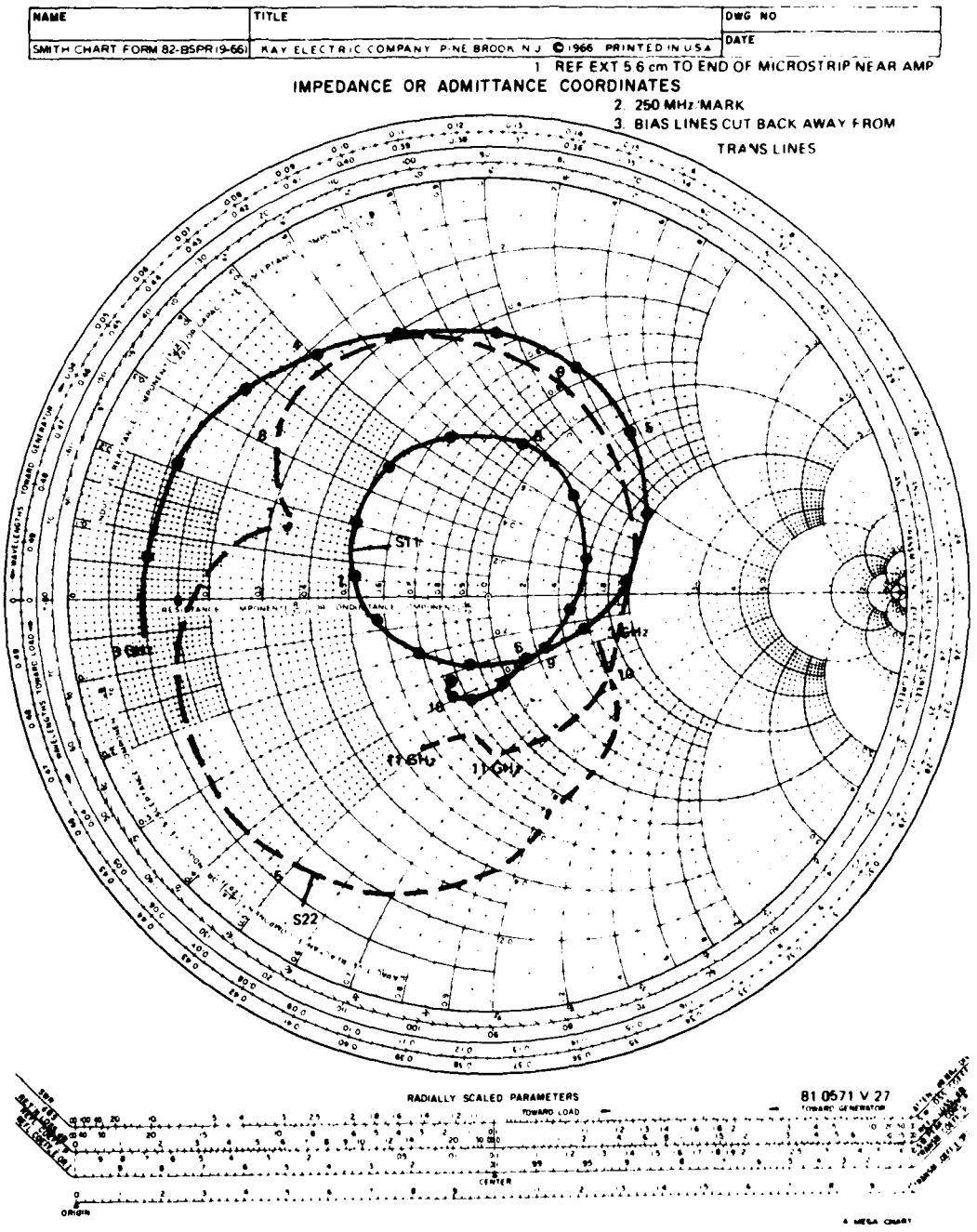
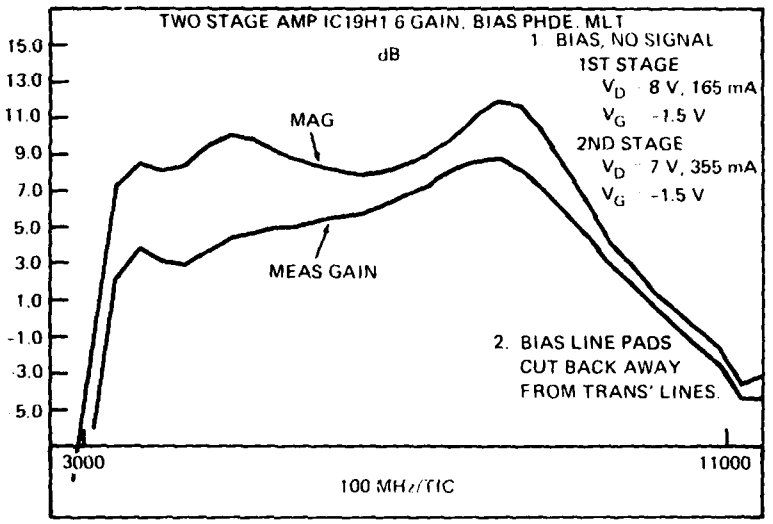
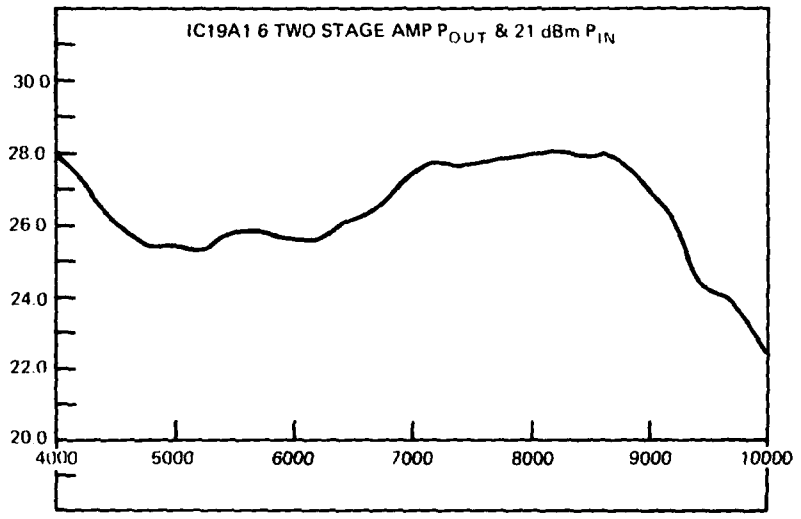


Figure 3-28. S_{11} for Mark III Amplifier



(A) SMALL SIGNAL



(B) LARGE SIGNAL

81 0571 V 28

Figure 3-29. Mark III Amplifier Response Curves

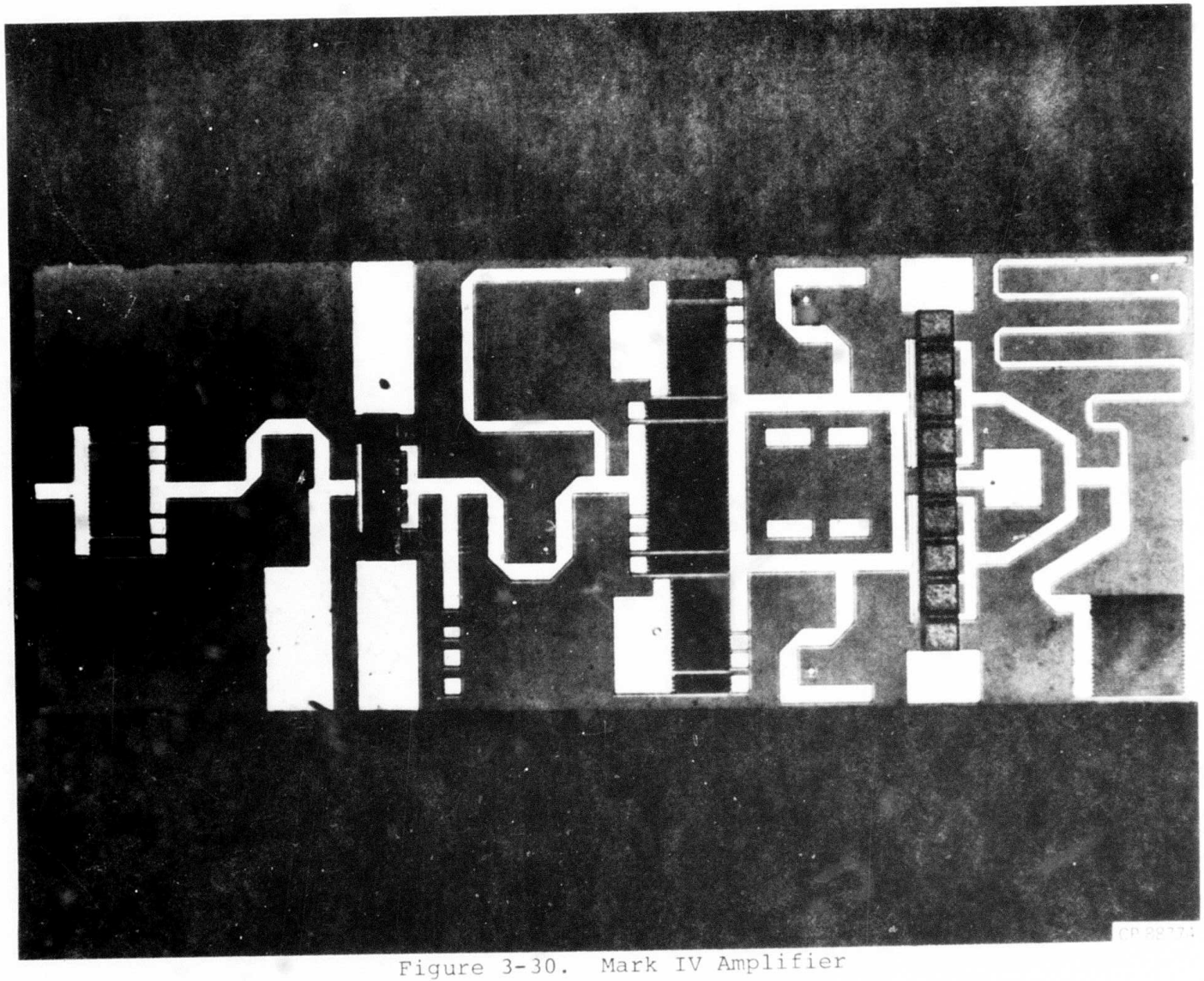


Figure 3-30. Mark IV Amplifier

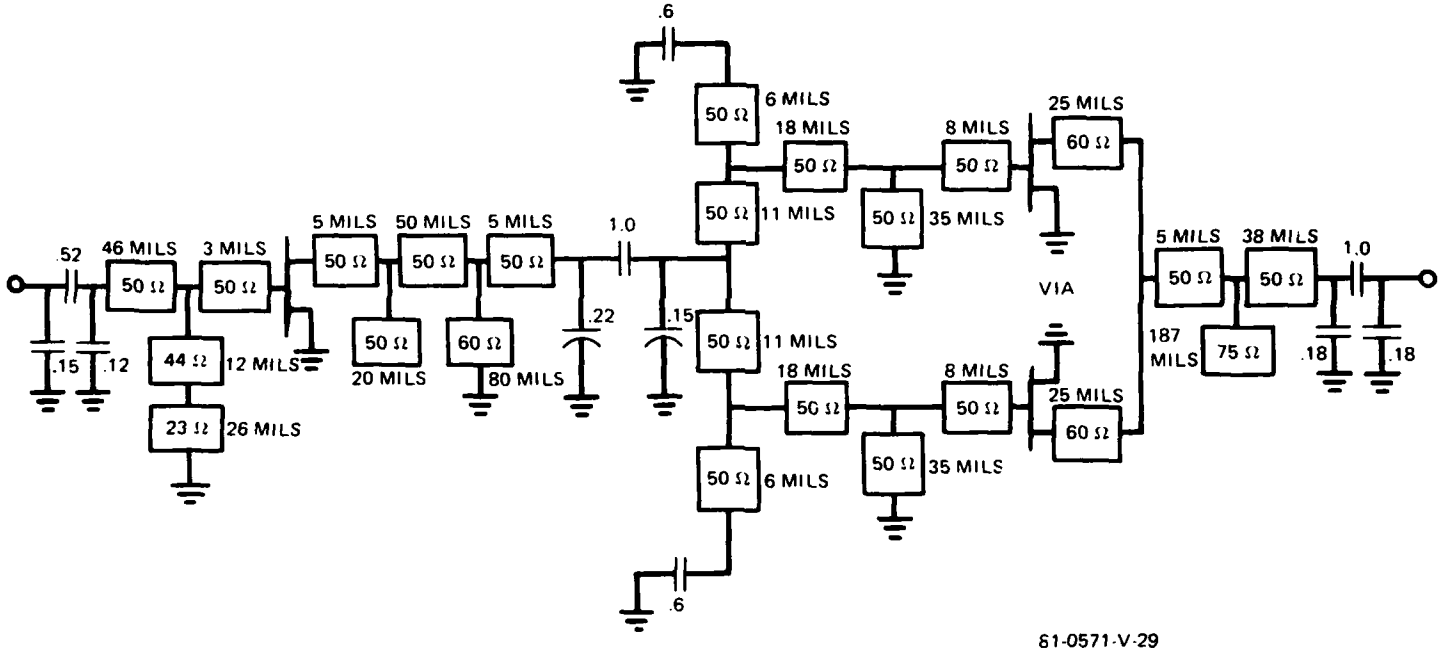


Figure 3-31. Mark IV Amplifier Schematic

This amplifier produced 28 ±0.7 dBm output from 5.7 to 11.0 GHz with 6 ±0.7 dB associated gain. The amplifier S_{11} and large signal frequency responses are shown in figure 3-32 and 3-33 respectively. The improved high frequency response confirmed the validity of the inclusion of the small gate inductance in the intrinsic FET model.

3.5.6 Mark V Amplifier

A fifth two-stage amplifier was in processing at the conclusion of this program. Several important circuit design advances were incorporated into this design. For the first time, load pull characterizations of the FETs were available over the full 5-10 GHz bandwidth. (Previous characterization extended from only 7-10 GHz due to equipment limitations.) The amplifier schematic is shown in figure 3-34.

A CAD technique for optimizing the impedance locus of the output and interstage circuits in relationship to the load pull contours was developed and utilized. The output circuit (or interstage circuit in the case of the first stage) presents an impedance locus designed to cross the constant power load pull contours in a manner to provide constant gain and power at each frequency. At a given frequency, an error function was defined as the absolute value of the distance on the Smith Chart between the load pull contour and the impedance point presented to the FET by the circuit. A Fletcher Powell minimization procedure was employed to reduce the value of the error function across the band, thus fitting the impedance locus to the constant power contours. Figure 3-12 and 3-13 in section 3.3 show the impedance loci resulting from using this circuit optimization technique.

The last circuit improvement was the replacement of the 900 μm input stage transistor with a larger 1200 μm transistor to drive the second stage more effectively. These design advances should ensure a 1 watt output over the 5-10 GHz band.

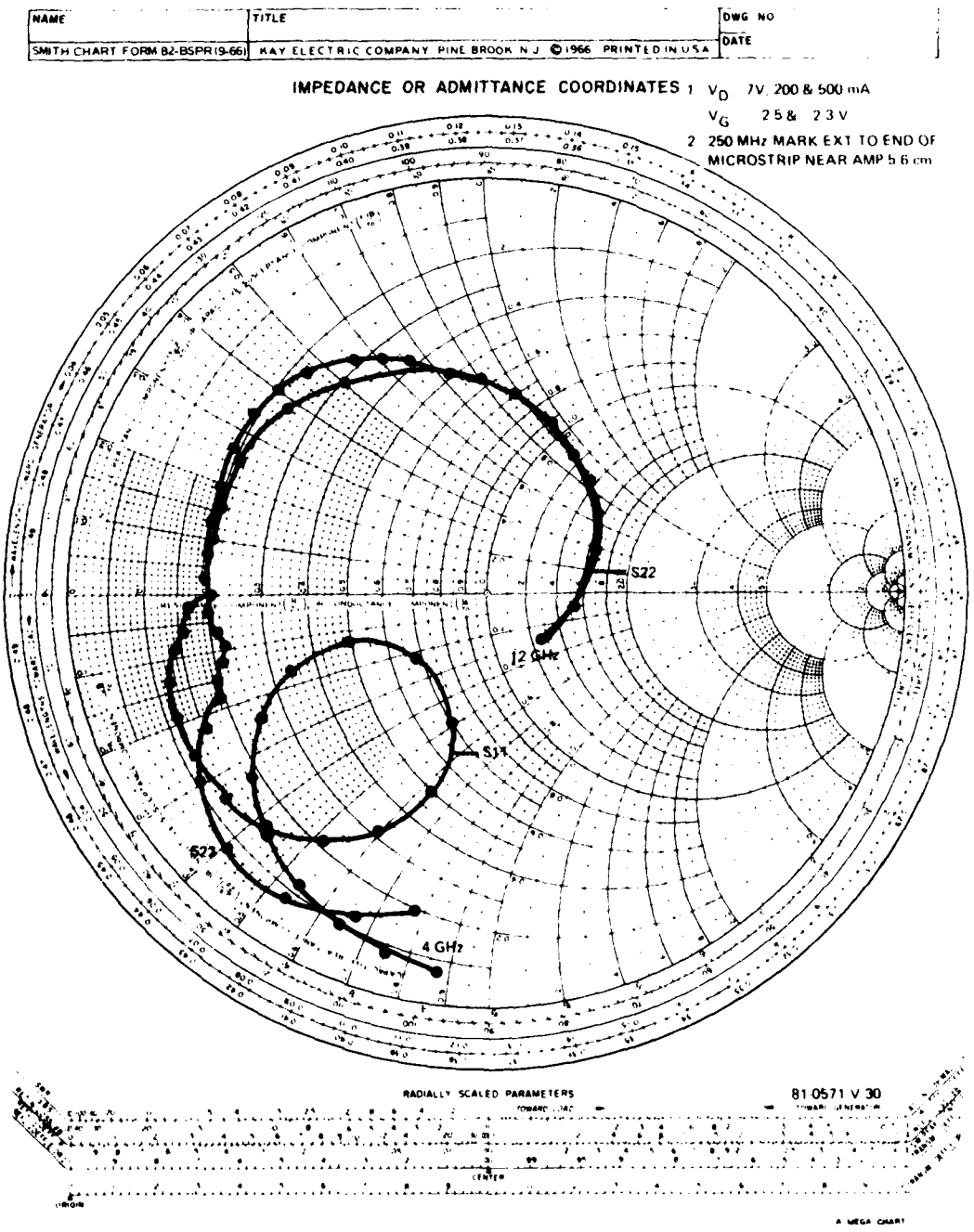


Figure 3-32. S_{11} for Mark IV Amplifier

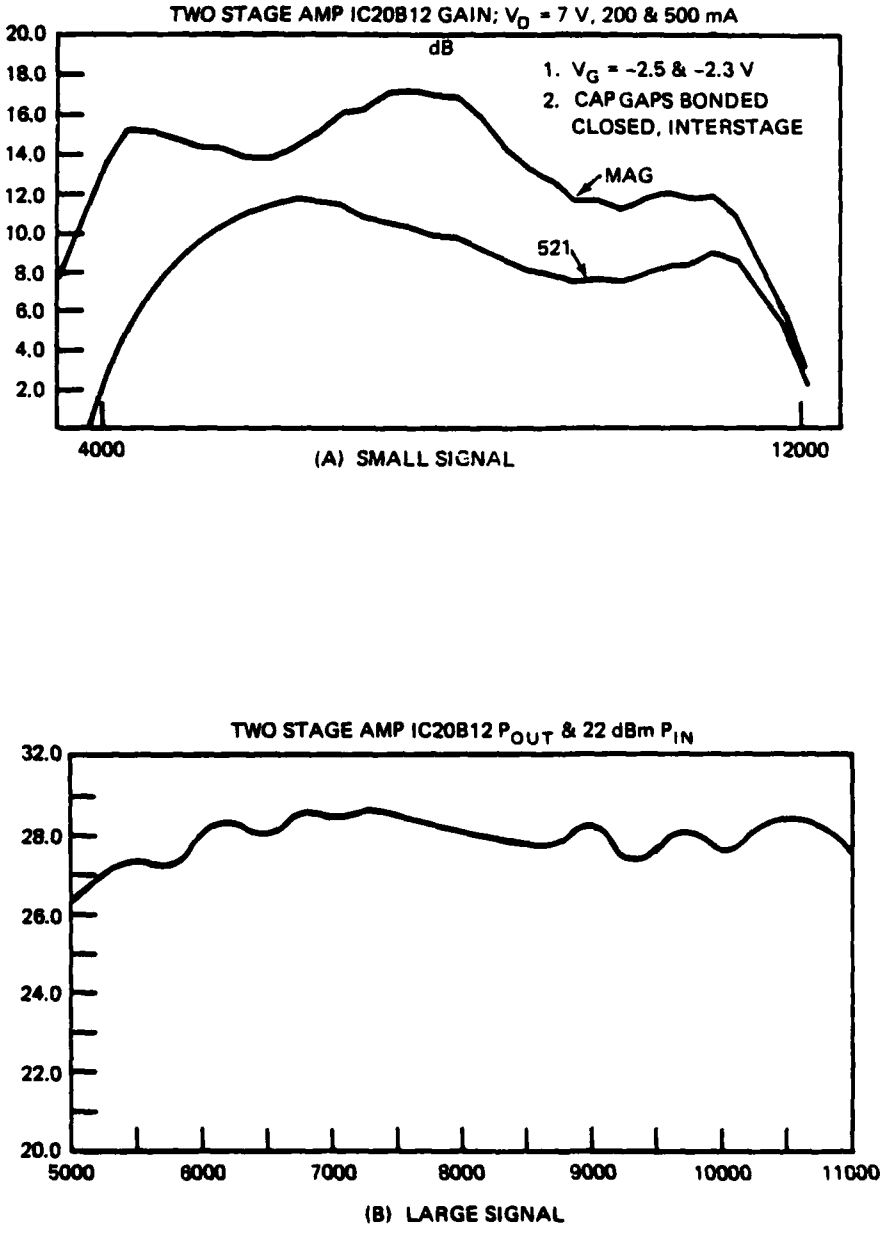


Figure 3-33. Mark IV Amplifier Gain Response

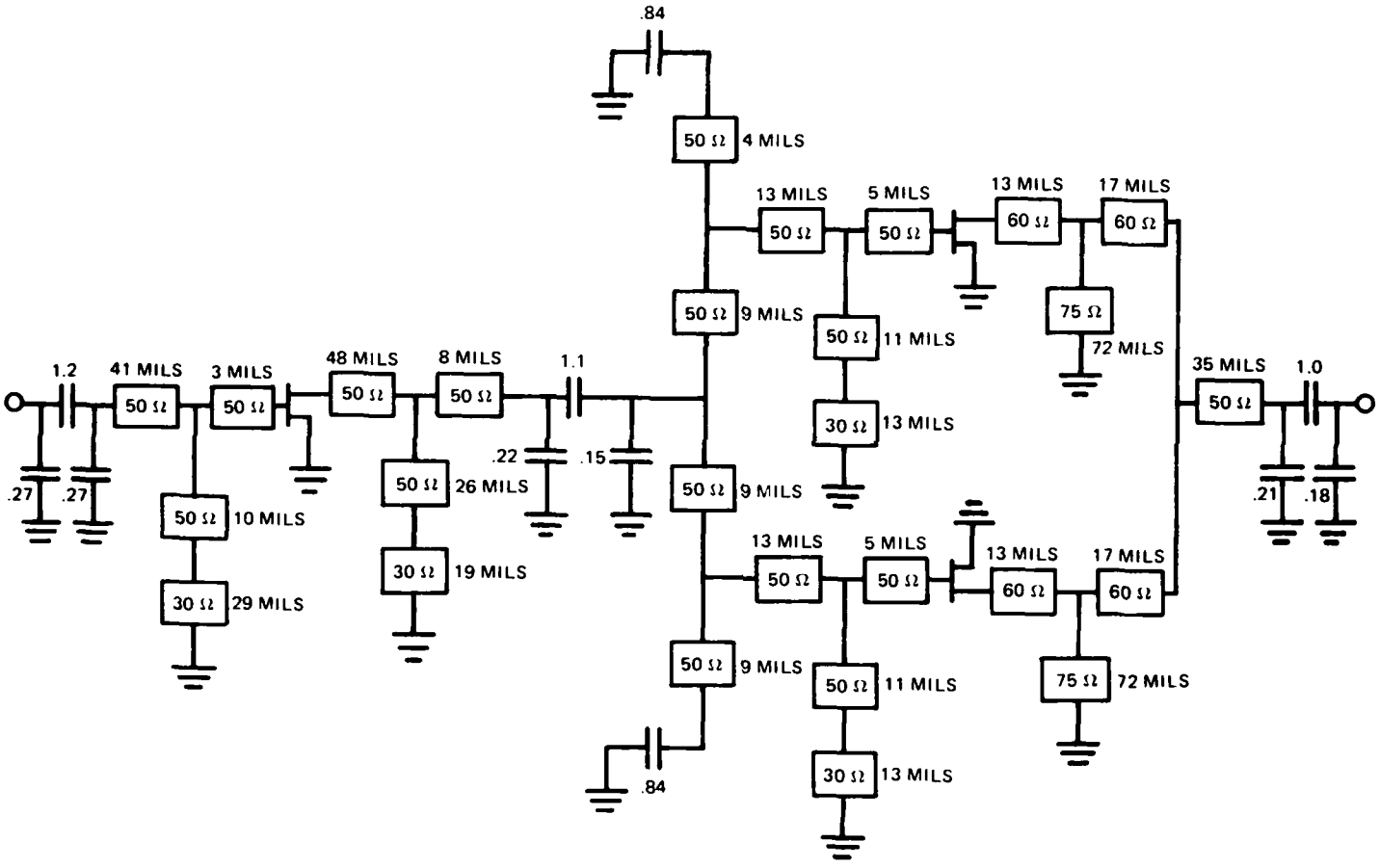


Figure 3-34. Mark V Amplifier Schematic

4. PHASE SHIFTERS

The high-pass, low-pass phase shifter has been the preferred mechanization for the three-bit phase shifter for this program because of its compact size and potential for wide-band operation.

In spite of this potential, however, it has proved to be nearly impossible to achieve octave band performance due to parasitic effects.

It was originally intended to fabricate the phase shifter monolithically using surface-oriented Schottky barrier diodes as switching elements. The use of Schottky barrier diodes, of course, would limit such a phase shifter to low level applications in the amplifier chain (typically a few milliwatts). Prior to fabricating a totally monolithic version, it was decided to fabricate a hybrid 90^{o} test bit using 5 micron chip diodes which would be bonded to the monolithic circuit elements of the phase shifter.

Such a hybrid 90^{o} test bit was fabricated and tested (see Progress report for the period September 30, 1978 - September 30, 1979, Report NR251-029-10, on this program) and suffered high insertion loss in the low pass state due to interaction of the reversed biased diode capacitance with the high-pass circuitry.

It was decided, due to the intensity of the amplifier effort, to postpone further fabrication efforts, in favor of a detailed analytic study of the phase shifter to see if alternate diode and/or circuit configurations would give the required octave band performance.

Studies during this reporting period showed that the insertion loss problem could be eliminated by using smaller, 2.5 micron junction diameter, diodes with their attendant small reverse biased capacitance. To study the phase shift performance of a 90^{o} bit using these small diodes, a monolithic microstrip circuit layout

was made, and all parasitic elements, such as the shunt capacitances of the interdigital capacitors, were accurately accounted for in the equivalent circuit model. Analysis of this accurate model showed excessive phase variation over the octave band as shown in figure 4-1. Attempts were made at circuit optimization to flatten the phase shift curve, but these were unsuccessful. The phase characteristic shown in figure 4-1, would of course be quite adequate for typical radar or communications systems bandwidths (up to 25%). To achieve octave band performance, further study of alternate high-pass low-pass configurations, such as 1) Low parasitic circuit layouts, and 2) Increases in the number of circuit elements in each configuration, must be performed. The analyses that were performed were for a 0.004" thick GaAs substrate as is required in order that the power amplifier's thermal impedance be adequately low. If, as is likely, the phase shifter operates at a much lower power level, it can be on a substantially thicker substrate which (1) reduces the parasitic shunt capacitance of all of the passive elements, (2) permits larger values of inductance for the same linewidth, and (3) reduces circuit losses. Further analysis with this added degree of freedom should be performed to evaluate the magnitude of the improvement and determine if thereby octave bandwidths can be achieved.

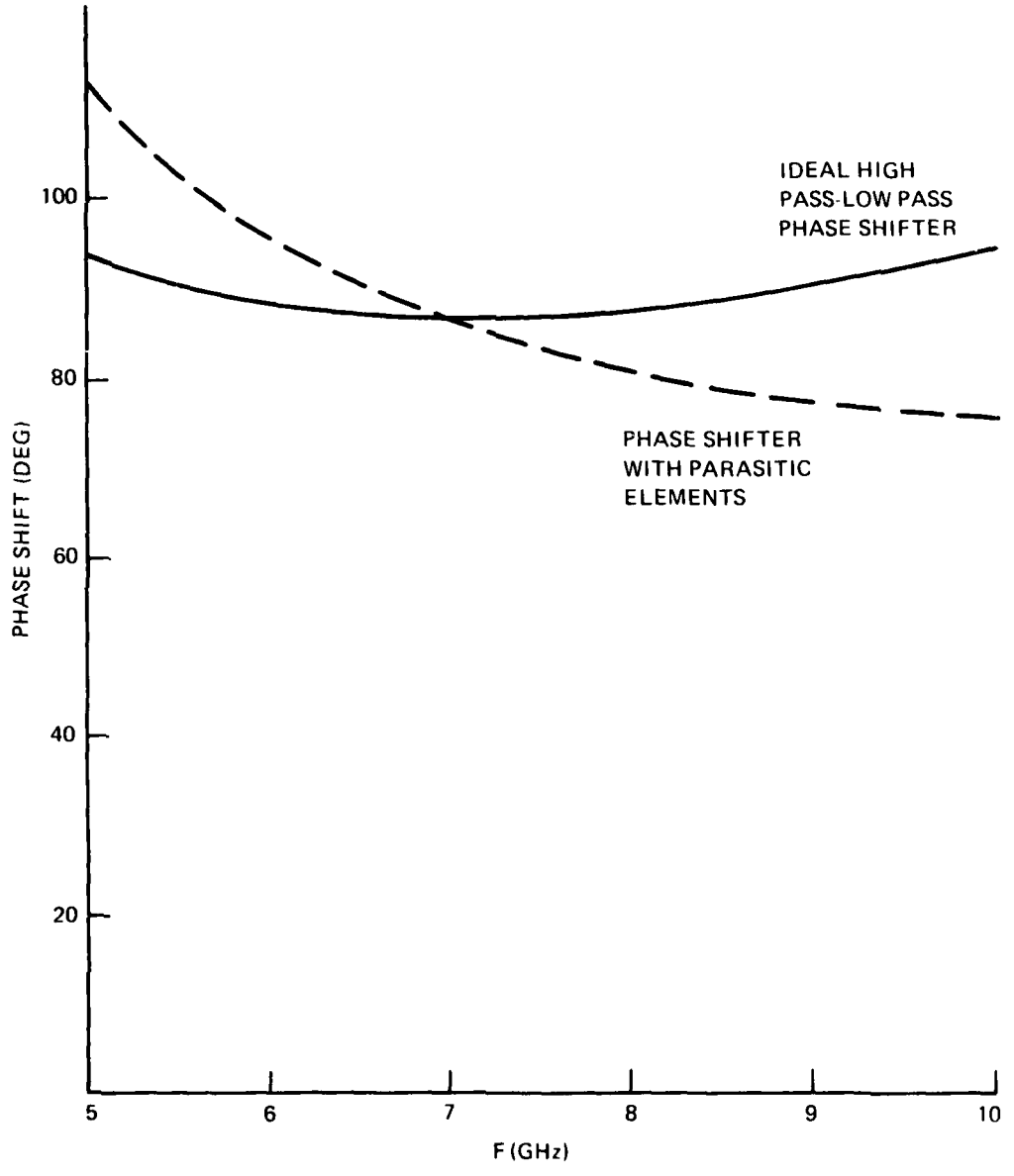


Figure 4-1. Phase Shift Performance

5. SUMMARY AND CONCLUSIONS

The major inpetus for the development of monolithic amplifiers on this program has been the promise of improved wideband performance due to the elimination of bond wires and other parasitic reactances normally associated with hybrid amplifiers and minimization of interconnecting line lengths. With the development of the two-stage monolithic amplifiers discussed earlier in this report, this promise of wideband performance has been fulfilled. This accomplishment has involved the development and marriage of a large number of technologies to produce a viable DSI^2 FET technology for GaAs monolithic amplifiers.

A summary of the specific technical achievements on this program includes:

- Use of High Purity GaAs Pyrotic Boron Nitride Boule Technology to provide the ultra-pure substrates required for the fabrication of these amplifiers (GaAs material developed on Westinghouse internal funds).
- The achievement of deep and shallow Si^+ selective implants over large 2" diameter wafers with high mobilities (5000 $cm^2/v.S$ at 10^{17} cm^{-3}). This technology eliminates the need for epitaxial growth and mesa etching, and eliminates step coverage problems.
- A FET fabrication technology capable of producing discrete FET's with output powers consistently between 0.60 and 0.70 W/mm with best values of 0.7 W/mm.
- The achievement of high Q interdigital capacitors accurately fabricated across 2" wafers.
- A design procedure for wide-band, high power monolithic amplifiers which includes sophisticated modeling of lumped elements, and extensive use of high power load pull characterization.
- Two-stage amplifiers with 28 dBm $\pm$0.7 dB output power from 5.7-11.0 GHz with 6 $\pm$7 dB associated gain, and 1 watt peak output power with narrow-band tuning.

Also, during the program, trimming has been proven to be a useful tool to facilitate development and reduce design time. Its utility in production should also be examined in the future.

In addition to interdigital capacitors, three other important amplifier technologies, vias, and air bridges, and thin film capacitors have been developed. To date, only interdigitated capacitors and vias have been incorporated since it has been found to be very important to phase in new technologies slowly so as not to seriously impact circuit yields.

Items for further study include:

- Yields - dc yields on present amplifiers have run as high as 40 percent. However, to accurately assess yields, many more runs are needed. A sequence of runs made on a pilot production basis would reveal faults and weak points in the processing and enable one to compile yield statistics for future production and cost planning.
- Phase Shifter - The high-pass - low-pass lumped element phase shifter has been shown not to be adequate for octave bandwidths when fabricated on thin (0.004") GaAs substrates. More study is required to ascertain if thicker substrates and/or alternate circuit configurations with more elements will give octave band performance.
- Incorporation of air bridges and thin film capacitors into future amplifier designs is essential.

APPENDIX A

GROWTH AND CHARACTERIZATION OF LARGE DIAMETER, UNDOPED SEMI-INSULATING GaAs FOR DIRECT ION IMPLANTED FET's

A.1 INTRODUCTION

High frequency GaAs MESFET's have received increasing attention over the past decade. Monolithically integrated power and low noise/high gain amplifiers operating at X-band frequencies, as well as high speed GaAs digital logic IC's, are now being developed at several laboratories throughout the world. Fabrication of these monolithic circuits by direct ion implantation of semi-insulating GaAs substrates is highly desirable because of its potential as a reliable, low-cost manufacturing technology. Significant progress is currently being made towards developing a viable planar ion implantation technology, but it is widely recognized that the variable, and often poor quality of semi-insulating substrates is a major limitation at present. GaAs substrates of high resistivity, which retain their semi-insulating properties throughout device fabrication are required, in order to maintain good electrical isolation for low-loss passive circuit elements and low parasitic capacitances associated with active devices. Unfortunately, at the temperatures normally employed in FET processing, the thermal stability of the semi-insulating substrate has often been a severe problem in the past. A common manifestation of the problem is the formation of a conductive surface layer following a thermal annealing process. In ion implantation technology, these anomalous conversion and compensation phenomena which have been observed following post-implantation annealing, adversely affect the implant profile and activation, and can result in poor control of full channel current and pinch-off voltage in directly implanted FET structures. It is probable that the high and variable concentrations of iron, chromium, oxygen and carbon impurities which are present

in typical Cr-doped semi-insulating GaAs substrates contibute to the difficulties in achieving uniform implant profiles, since these impurities can modify their electrical role or redistribute as a result of implantation and thermal annealing. Chromium redistribution has been graphically demonstrated in the case of directly implanted Cr-doped substrates.[1] In addition, typical Cr-doped GaAs substrates contain at least 1×10^{17} cm^{-3} ionized impurities which severely reduce the electron mobility in directly implanted FET channels and degrade the FET performance and frequency limitations. Thermally stable, high resistivity GaAs substrates containing very low concentrations of residual impurities are therefore highly desirable for direct ion implantation device fabrication.

To address the problem of unpredic properties associated with the semi-insulating GaAs substrates which are available commercially today, a crystal growth facility which utilizes a Melbourn Liquid-Encapsulated Czochralski (LEC) pullter has recently been established at our laboratories. LEC growth was selected over other growth technologies because of its current capability for producing two- and three-inch diameter <100>- and <111>-crystals of semi-insulating GaAs from which round, large-area substrates can be prepared (figure A-1). In device processing, handling and processing costs are approximately independent of wafer size, making large-area substrates very attractive for future, low cost manufacturing technology. Perhaps of even more significance is the adaptability of LEC growth to silicon-free, pyrolytic boron nitride crucible techniques,[2,3] offering the potential of semi-insulating GaAs crystals of significantly improved purity, without resorting to intentional Cr doping.

In this appendix, we report the growth of high purity, two- and three-inch diameter <100> -GaAs crystals pulled from pyrolytic boron nitride crucibles and the characterization of these substrates for direct ion implantation device fabrication. These updoped GaAs/PBN crystals consistently exhibit resistivities

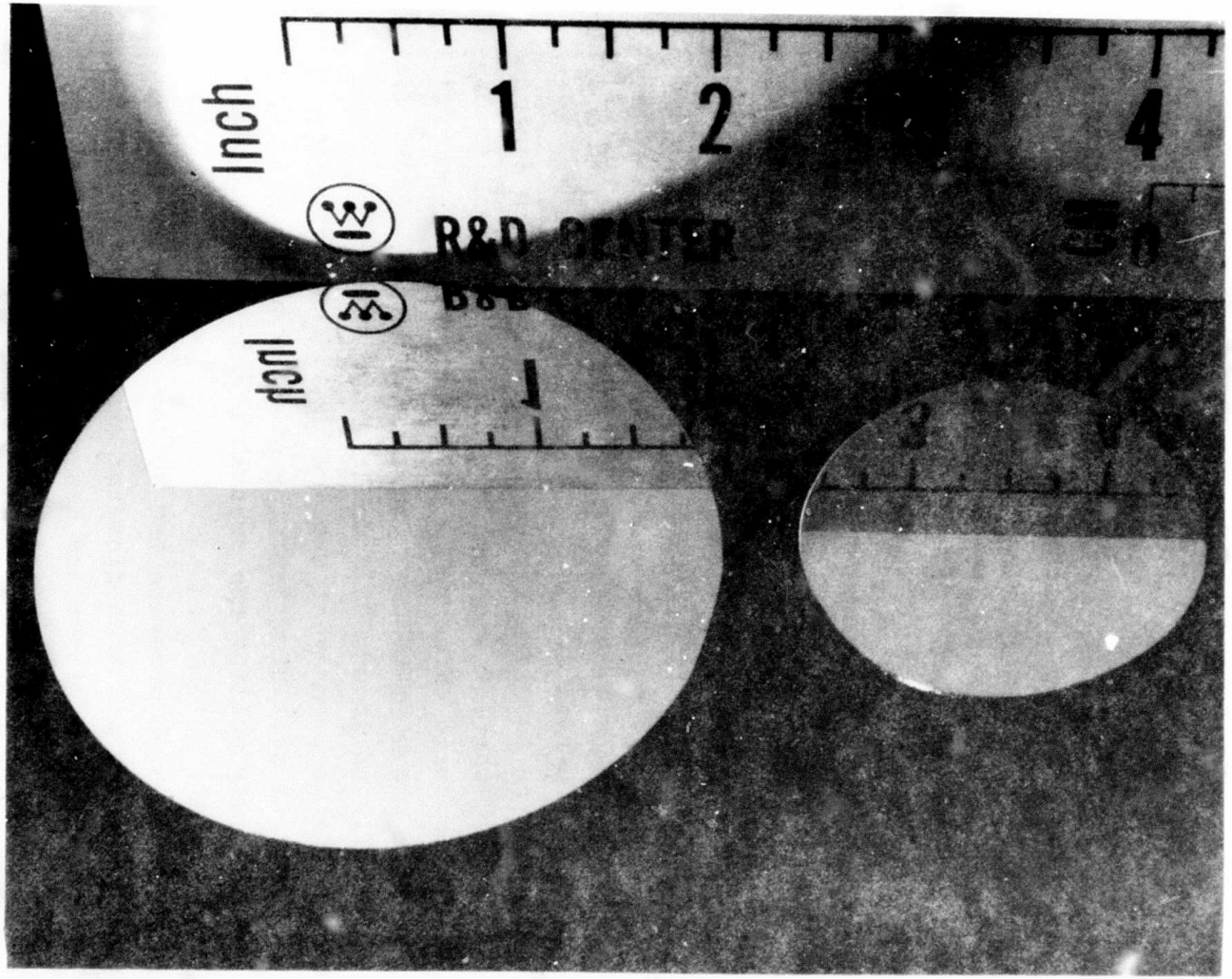


Figure A-1. Two- and Three-Inch Diameter GaAs Wafers Cut From <100>- Axially Oriented Crystals Pulled in a Melbourn Liquid Encapsulated Czochralski Puller.

approaching 10^8 ohm cm, are thermally stable under implantation annealing and contain very low total impurity concentrations. The residual silicon and chromium contents are in the low 10^{15} cm^{-3} range. The improved crystal purity contributes significantly to the high channel mobility (approaching 5,000 $cm^2/Vsec$ at 1×10^{17} cm^{-3} peak donor concentrations of interest for power FET structures) and the uniform, reproducible implant profiles which have been achieved in directly implanted GaAs/PBN substrates. Discrete FET's and monolithic amplifier circuits fabricated on these substrates exhibit excellent transconductances, small signal gains and RF output power at X-band frequencies.

A.2 CRYSTAL GROWTH

Liquid-Encapsulated Czochralski (LEC) growth was first demonstrated experimentally in 1962 by Metz et al.[4] for the growth of volatile PbTe crystals, and has since been developed by Mullin et al.[5] for several III-V crystals. In this Czochralski technique, the dissociation of the volatile As from the GaAs melt which is contained in a crucible is avoided by encapsulating the melt in an inert molten layer of boric oxide and pressurizing the chamber with a non-reactive gas, such as nitrogen or argon, to counterbalance the As dissociation pressure. In-situ compound synthesis can be carried out from the elemental Ga and As components since the boric oxide melts before significant sublimation starts to take place ($\approx 400^{\circ}C$). Compound synthesis occurs rapidly and exothermally at about $820^{\circ}C$ under a sufficient inert gas pressure ($\approx$30 atm) to prevent sublimation of the arsenic component. Crystal growth is initiated from the stoichiometric melt by seeding and slowly pulling the crystal through the transparent boric oxide layer.

The Melbourn high pressure LEC puller[6] used in this work is a resistance-heated six-inch diameter crucible system capable of charges up to 8-10 kg weight and can operate at pressures up to 150 atmospheres. The system features a closed-circuit TV for

viewing the melt and a differential crystal weight monitor for diameter control.

A number of 2- and 3-inch diameter <100> -GaAs crystals free of major structural defects such as twin planes, inclusions and precipitates have been grown successfully. A photograph of two <100> -GaAs crystals each weighing approximately 3 kg is shown in figure A-2. To achieve reproducible growths of high quality, twin-free crystals, a growth procedure was adopted which included the use of vacuum baking of the boric oxide encapsulant to remove residual moisture - an important factor in maintaining high visibility of the melt-crystal interface during growth, and the gradual increase of the crystal diameter to the desired value during the initial stages of growth (as seen in the crystal displayed on the right-hand side of figure A-2) to minimize dislocation generation. Semi-insulating GaAs crystals have been prepared from undoped and Cr-doped melts synthesized in-situ from high purity elemental arsenic and gallium charges and contained in both fused silica and pyrolytic boron nitride crucibles. Selected semi-insulating GaAs crystals have been sawed and polished to provide substrates for device fabrication. Selection of both Cr-doped and undoped crystals was based on structural, chemical and electrical characterizations which are described below.

A.3 SUBSTRATE QUALITY

A.3.1 Crystalline Perfection

It has been shown on an experimental basis that crucible-pulled GaAs crystals can be grown free of dislocations at small crystal diameters, usually ≤ 0.5 in and crystal lengths <3 in.[7] For these small crystals, successful dislocation-free growth depends upon the following growth conditions: (1) a Dash-type seeding method in which the seed is grown with a thin neck before increasing the diameter to form the crystal cone[8]; (2) a melt which is close to stoichiometry and a small axial temperature gradient at the interface[9]; (3) the growth interface maintained flat to convex toward the melt.[10] In addition, the angle of the crystal

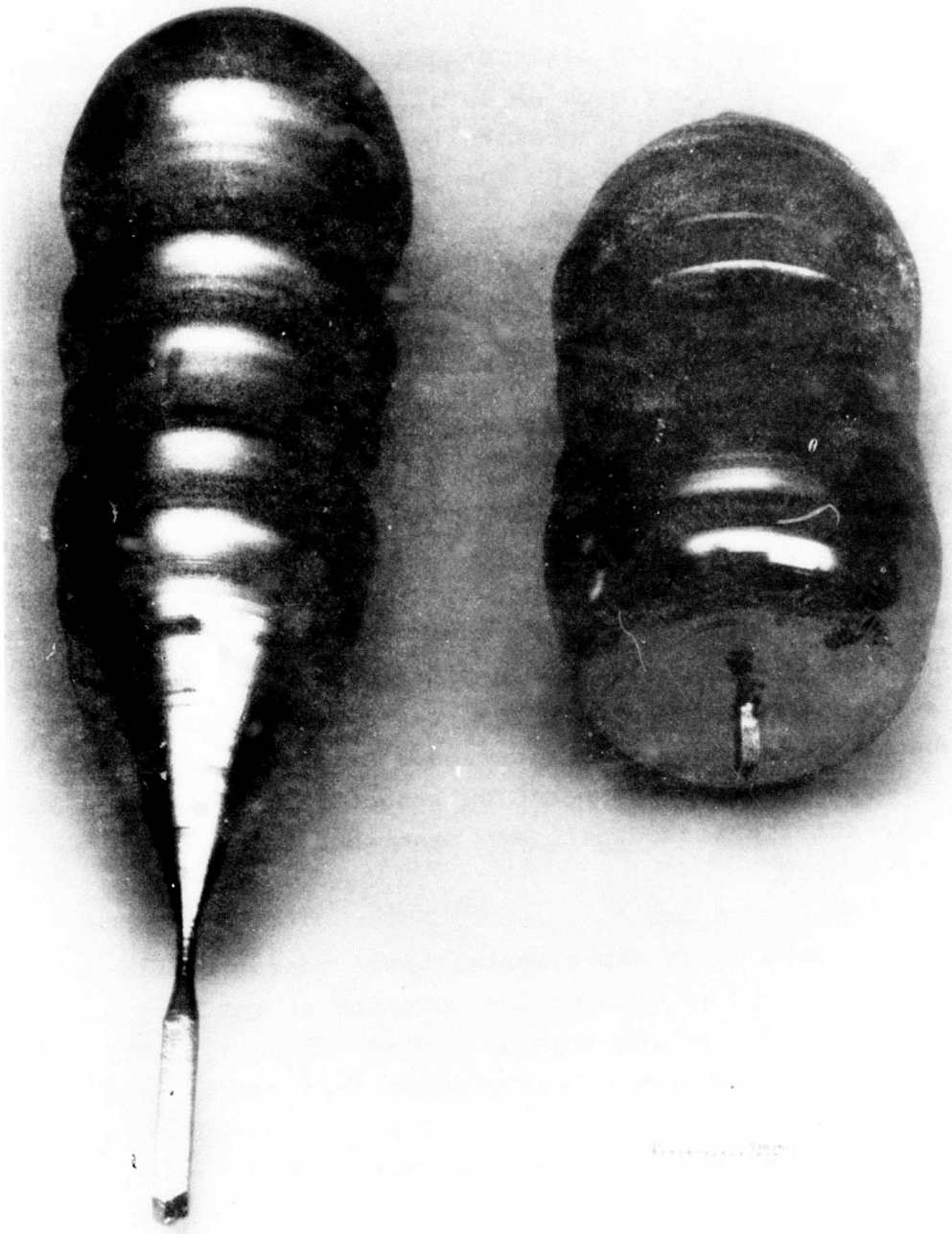


Figure A-2. Two- and Three-Inch Diameter, <100> -Axially Oriented GaAs Crystals Grown by LEC Pulling From Six-Inch Diameter Pyrolytic Boron Nitride Crucibles

cone is also important for dislocation-free growth. If the cone angle is too large, dislocation generation can result from the high internal stresses which develop as the crystal cone emerges from the B_2O_3 encapsulant.[11]

Although large diameter (≤3 in) LEC GaAs crystals grown in the <100> axial orientation are free of gross structural imperfections, such as twins and inclusions, these crystals are usually characterized by high background densities of dislocations (10^4 to 10^5 cm^{-2}), such as shown by the x-ray reflection topograph of figure A-3 for a typical <100> LEC GaAs wafer. Our preliminary investigations on improving the structural quality of large diameter GaAs crystals have concentrated on determining the optimum conditions for initiating dislocation-free growth. Figure A-4(a) and (b) show x-ray reflection topographs of longitudinal sections of seed-and cones for two <100> GaAs crystals corresponding to two different cone angles: (a) a relatively shallow cone and (b) a steeper cone of 27" to the crystal axis. In both cases dislocation-free growth is initiated using a Dash-type seeding. As the cone diameters increase, the dislocation densities increase, particularly in the crystal interior, together with activation of glide planes; however, the rate of dislocation multiplication has been reduced by the steeper cone angle (figure A-4b).

A.3.2 Impurity Content

Secondary ion mass spectrometry bulk analysis[12] of LEC GaAs material pulled from both quartz and pyrolytic boron nitride crucibles at our laboratories, as well as large-area boat-grown substrates purchased from an outside supplier have been carried out. A wide range of impurity species were examined and the data clearly show that the lowest impurity content is achieved in LEC growths from PBN crucibles. Quantitative estimates of impurity concentrations were obtained by calibration against GaAs samples which had been ion implanted with known doses of specific impurities. The results are shown in figure A-5 where the markers

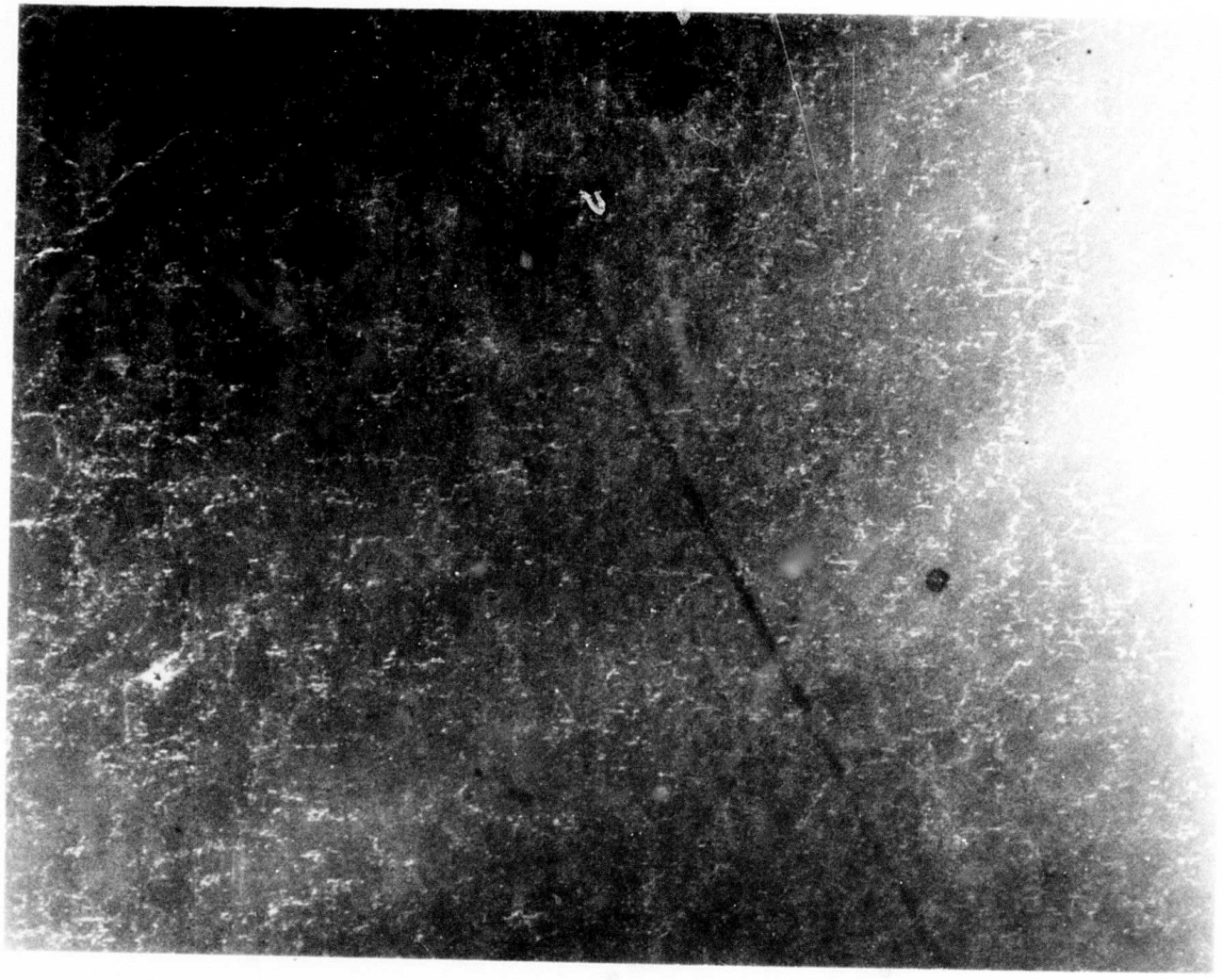


Figure A-3. Reflection X-Ray Topograph ($\alpha = <315>$) of LEC Grown GaAs Substrate Pulled From Boron Nitride Crucible.

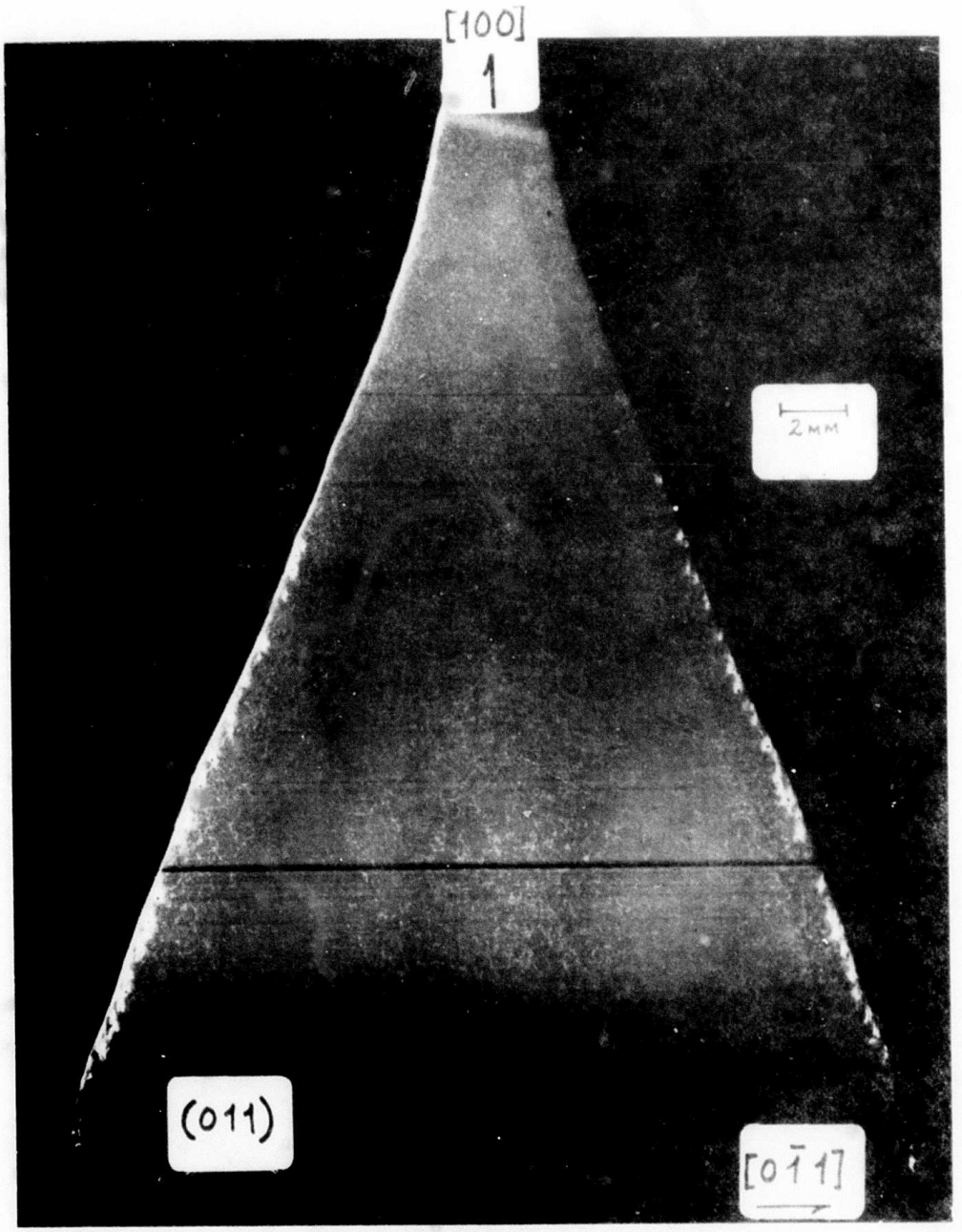


Figure 4-a. Reflection X-Ray Topograph (g = <315>) of (011) Longitudinal Section for a Shallow Cone Angle. Crystal Pulled From Pyrolytic Boron Nitride Crucible.

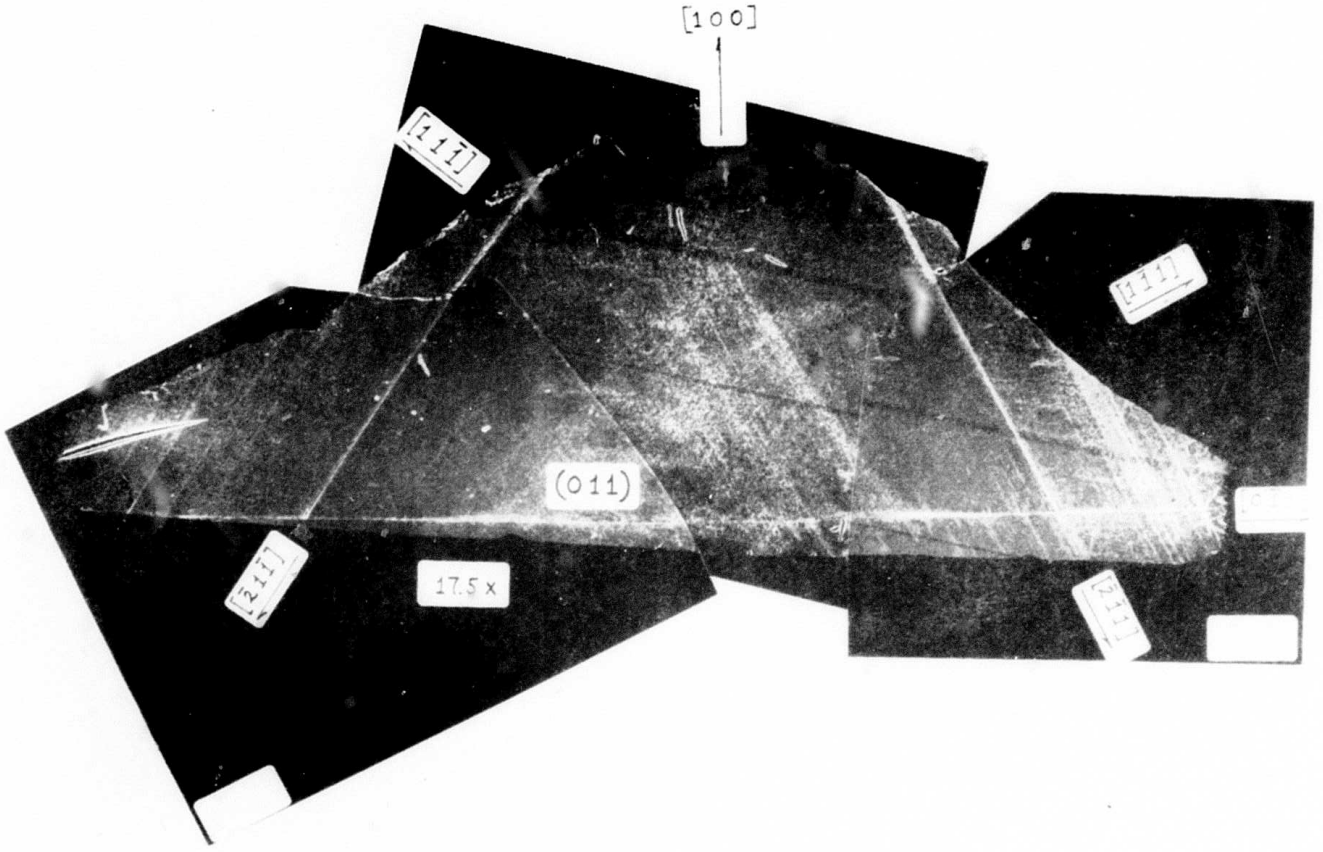


Figure A-4b. Reflection X-Ray Topograph (g = <260>) of (011) Longitudinal Section for Cone Angle of 27°. Crystal Pulled From Pyrolytic Boron Nitride Crucible.

Curve 720876-A

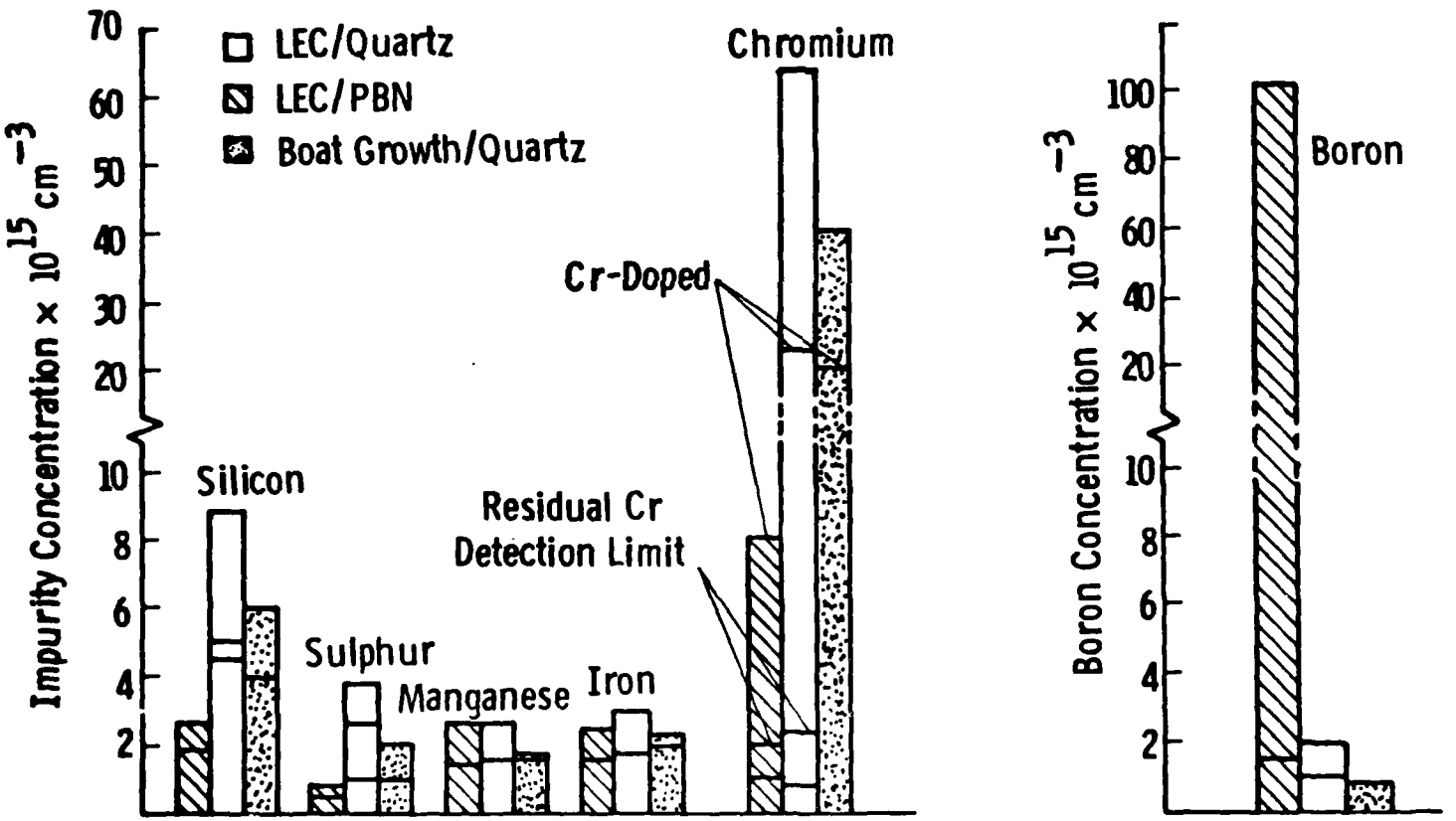


Figure A-5. Bulk SIMS Analysis of Semi-Insulating GaAs Prepared by LEC & Horizontal Bridgeman Growth. Horizontal Markers Indicate Different Crystal Samples.

on each bar represent data for different crystals. Residual silicon concentrations in the (1 to 2) x 10^{15} cm^{-3} range are observed in GaAs/PBN samples compared to levels which range up to 10^{16} cm^{-3} in crystals grown in quartz containers. The residual chromium content in undoped LEC GaAs crystals pulled from either PBN or fused silica crucibles is below the detection limit of the SIMS instrument, estimated to be in the 1 - 2 x 10^{15} cm^{-3} range. Analyses of LEC-grown crystals pulled from Cr-doped melts reveal that the Cr content (typically 2 x 10^{16} cm^{-3} at the seed-end and approaching 10^{17} cm^{-3} at the tang) is close to the anticipated doping level based on the amount of Cr dopant added to the melt and its reported segregation behavior.[13] Cr dopant levels of (2 to 4) x 10^{16} cm^{-3} were observed in the boat-grown samples. The reduced concentration of shallow donor impurities in growths from PBN crucibles permits lower Cr doping levels to be utilized, as shown in figure A-5 where 8 x 10^{15} cm^{-3} Cr dopant concentration is observed in a sample cut from near the tang end of the crystal.

Additional SIMS studies[14] indicate that LEC growths from PBN crucibles generally result in high boron concentrations (10^{17} cm^{-3} range) in the GaAs material versus low 10^{15} cm^{-3} concentrations in quartz crucible growth. No significant differences in carbon 10^{17} cm^{-3}, oxygen 10^{16} cm^{-3}, selenium $<10^{15}$ cm^{-3} and tellurium $<10^{15}$ cm^{-3} contents of different GaAs samples are revealed by these investigations. The results reported in section 4 suggest that the 10^{17} cm^{-3} concentrations of boron and carbon in GaAs/PBN substrates remain electrically neutral through implantation processing and do not contribute significantly to ionized impurity scattering.

A.3.3 Electrical Characterization

Resistivity and thermal stability measurements were carried out on LEC-grown GaAs substrates to determine the suitability of the substrates for ion implantation studies. Additional assessment of the substrate quality was provided by measurements of the

transport properties of n-doped layers formed by direct ion implantation into the substrate.

The axial resistivity variation along undoped and Cr-doped GaAs crystals is shown in figure A-6. Substrate resistivities in the 10^8 - 10^9 ohm cm range are observed in Cr-doped substrates (containing high 10^{16} cm^{-3} Cr concentrations) compared to resistivities of 10^7 to 10^8 ohm cm in undoped GaAs/PBN substrates. Lightly Cr-doped GaAs/PBN crystals (8 x 10^{15} cm^{-3} Cr content) exhibit resistivities greater than 3 x 10^8 ohm cm. Undoped GaAs crystals pulled from fused silica crucibles show lower resistivity-ties and a greater variation along the crystal. Variable results were obtained from crystal to crystal, varying from 10^6 to 10^7 ohm cm in one to resistivities in the 10^3 ohm cm in another crystal.

The mechanism of electrical compensation in semi-insulating GaAs has been studied extensively[15,16] and it has been tacitly accepted that semi-insulating behavior in undoped GaAs results from oxygen compensation - an impurity which is introduced to suppress silicon contamination from dissociation of the SiO_2 ampoule in horizontal Bridgeman growth and is unintentionally incorporated in LEC grown crystals. In Cr-doped GaAs, high resistivity is believed to result from the compensation of shallow donors by the deep chromium acceptors. More recently, Zucca[16] has proposed a model which includes both a deep acceptor (Cr) and deep donor (oxygen) to interpret experimental resistivity data in lightly Cr doped GaAs (5 x 10^{15} cm^{-3} Cr). The assignment of the measured deep donor level at about 0.66 to 0.72 eV from the conduction band edge is however controversial.[17] Zucca's data indicate predominantly hole conduction from chromium acceptors (E_c - 0.83 eV) in highly Cr-doped substrates (6 x 10^{16} cm^{-3} Cr).

Plots of log resistivity versus reciprocal temperature for undoped and Cr doped LEC GaAs crystals pulled from pyrolytic boron nitride and fused silica crucibles are shown in figure A-7. All the samples measured showed conduction by electrons to be

Curve 720821-A

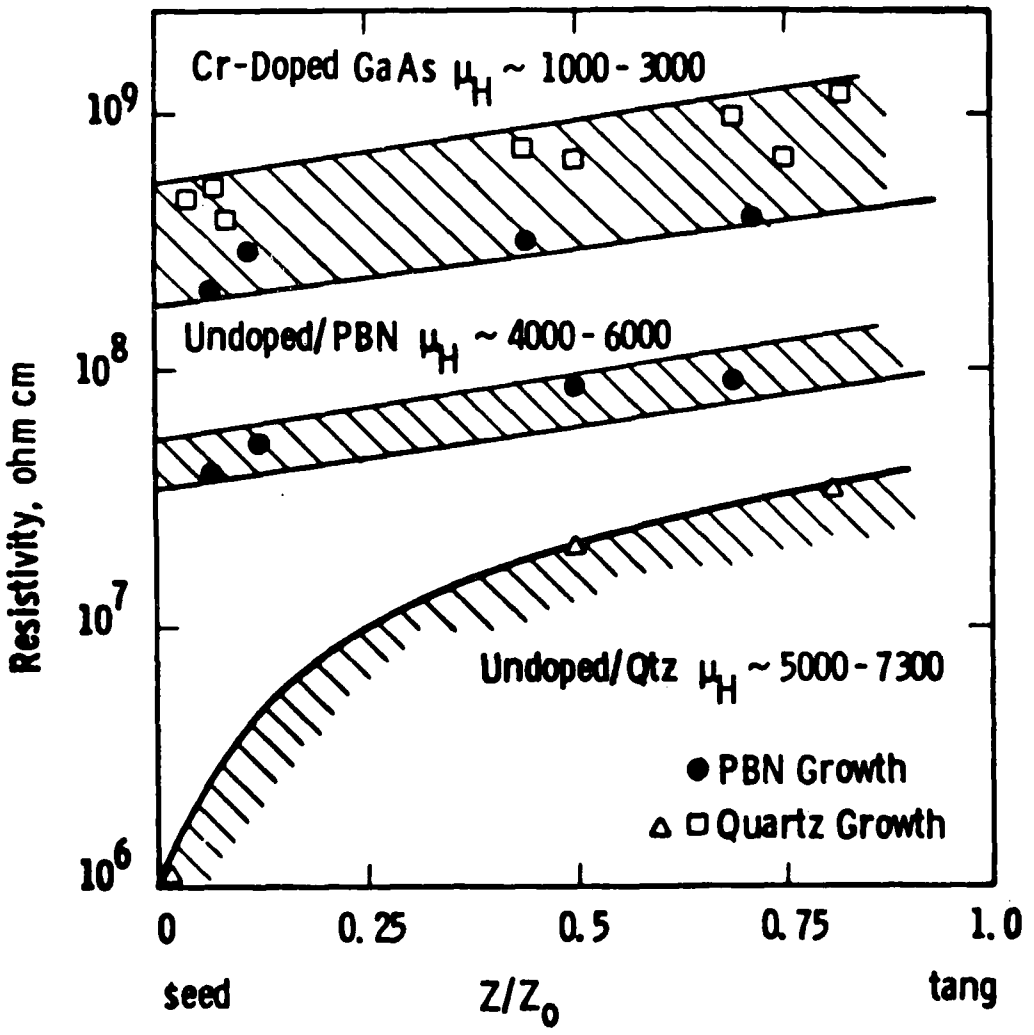


Figure A-6. Axial Resistivity Variation Along LEC Grown GaAs Crystals Pulled From Quartz and Pyrolytic Boron Nitride Crucibles.

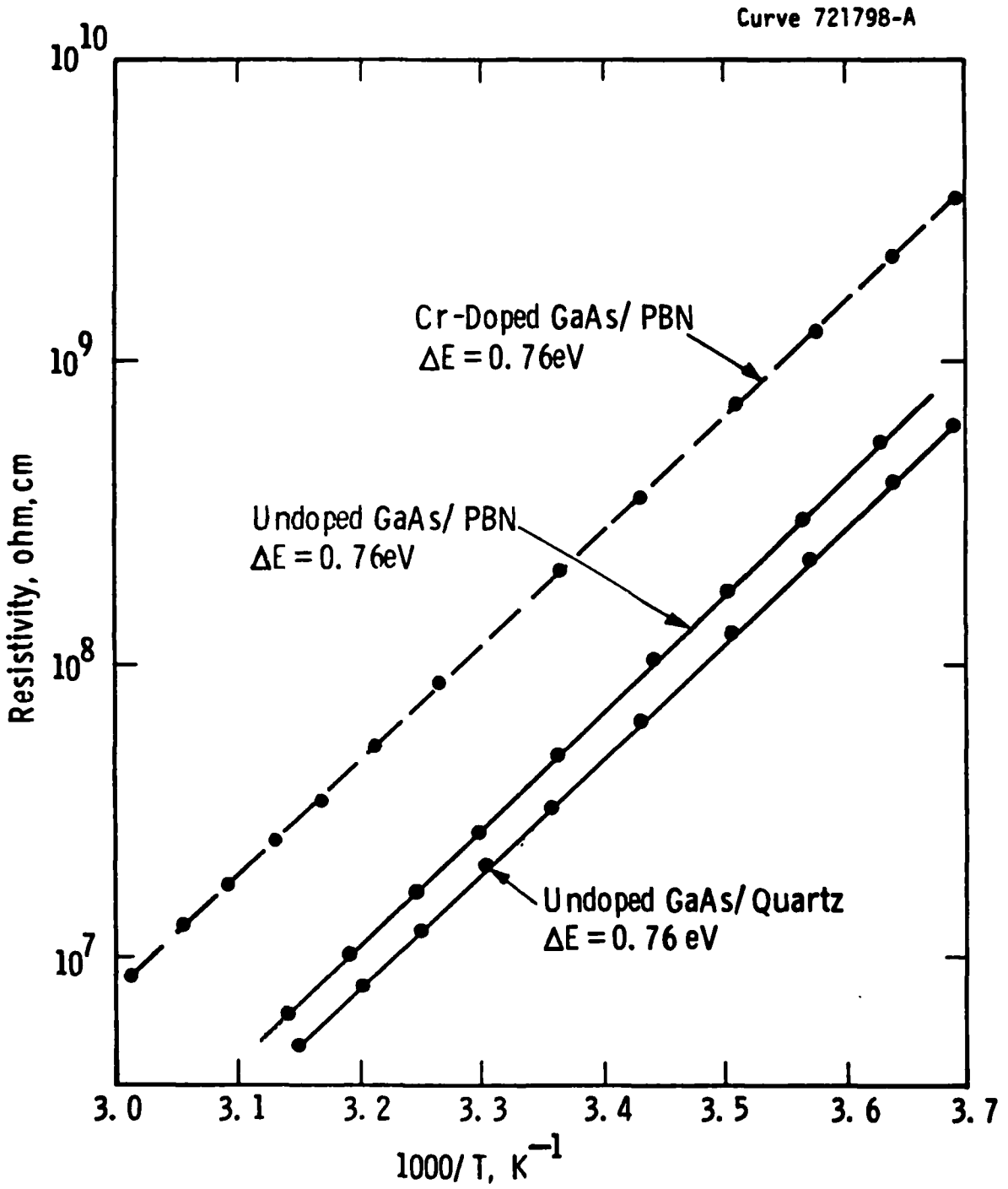


Figure A-7. Log Resistivity as Function of Reciprocal Temperature for LEC GaAs Grown in PBN and Quartz Crucibles.

dominant and independent of the Cr content between 2×10^{15} and 8×10^{16} cm^{-3}. An activation energy of 0.76 eV was measured for all sample types. While these results confirm the importance of the deep donor level observed by others in semi-insulating GaAs, no other conclusions can be drawn at present and further studies are in progress.

Although direct evaluation of the carrier mobilities and net donor and acceptor concentrations in semi-insulating GaAs substrates is made difficult by the high sample impedance and the complexity of data interpretation,[17] high impedance Hall measurements performed at ambient temperature indicate high apparent electron mobilities of between 5,000 and 7,200 cm^2/vsec in undoped GaAs pulled from quartz or PBN crucibles and is a qualitative indication of the high purity of these samples. In contrast, the measured electron mobilities in all semi-insulating Cr-doped samples are in the 1,000 to 3,000 cm^2/vsec range.

Thermal stability of substrates for ion implantation was assessed by means of resistivity measurements following an encapsulated anneal of the semi-insulating slice (prior to implantation) to determine whether any conducting surface layers have formed as a result of thermal treatment. Samples for the unimplanted, encapsulated anneal test were prepared using the same process as is used for implantation. Wafers are prepared by etching to remove cutting damage and bromine-methanol polishing on the front surface to 0.020 in thickness. A 900Å layer of Si_3N_4 was deposited on the front surface by a plasma-enhanced silane-nitrogen reaction. These depositions were performed in a modified LFE PND301 reactor at a substrate temperature of 340°C, nominal gas flows at 40 ccm 1-1/2% SiH_4 in Ar and 3 sccm N_2, and 100 watts RF power, which yielded 75 Å/min deposition rates. A 2500Å thick layer of 7% phospho-silicate glass was also deposited at 420°C on both surfaces prior to annealing as protection against pinholes in the nitride encapsulant (and is also utilized for pattern definition with selective implants in FET processing). The wafers are

annealed at 860°C for 15 minutes in a forming gas atmosphere. Surface sheet resistances exceeding 10^6 ohms/□ are desired after annealing to ensure isolation of passive as well as active elements in analog IC processing.

Typical sheet resistance data for semi-insulating undoped and lightly Cr-doped GaAs/PBN substrates and conventionally Cr-doped GaAs substrates before and after encapsulated anneals are shown in figure A-8. Some degradation in the sheet resistance is always observed as a result of the thermal treatment, but the leakage currents measured in these low field measurements (10^3 v/cm) and the RF losses observed in monolithic circuits fabricated on these substrates are low. In particular, surface leakages of <30 μA at 15 volts bias and high breakdown voltages of 25 volts were measured in interdigitated capacitor structures (5 μm separation and 13.2 mm periphery) to test the performance under the high operating fields normally utilized in monolithic circuits.[18]

A.4 ION IMPLANTATION

Direct ion implantation of undoped and Cr-doped GaAs substrates was performed at ambient temperature using ^{29}Si ions in a 400 keV Varian/Extrion ion implanter. The Si beam was generated from a SiF_4 source so that the Si isotope ratios could be measured and $^{29}Si^+$ beam purity assured. The implants discussed here were performed through a 900Å thick front surface Si_3N_4 encapsulation. Separate sequences of bare implants indicate that the activation efficiency and mobility data are identical in both cases. High sensitivity SIMS profiles of ^{29}Si and ^{52}Cr after a 4×10^{12} cm^{-2} - 350 keV $^{29}Si^+$ implant through Si_3N_4 is shown in figure A-9. These specimens received the standard PSG overlay and 860°C/15 minute anneal. In figure A-9, the surface ^{29}Si and ^{28}Si peaks are probably the result of matrix effects in the SIMS measurements and recoil implantation from the Si_3N_4 layer. The effects of recoil implantation are not detected in electrical measurements because of surface depletion phenomena. Surface accumulation of Cr in both Cr-doped and undoped LEC GaAs substrates is typical of

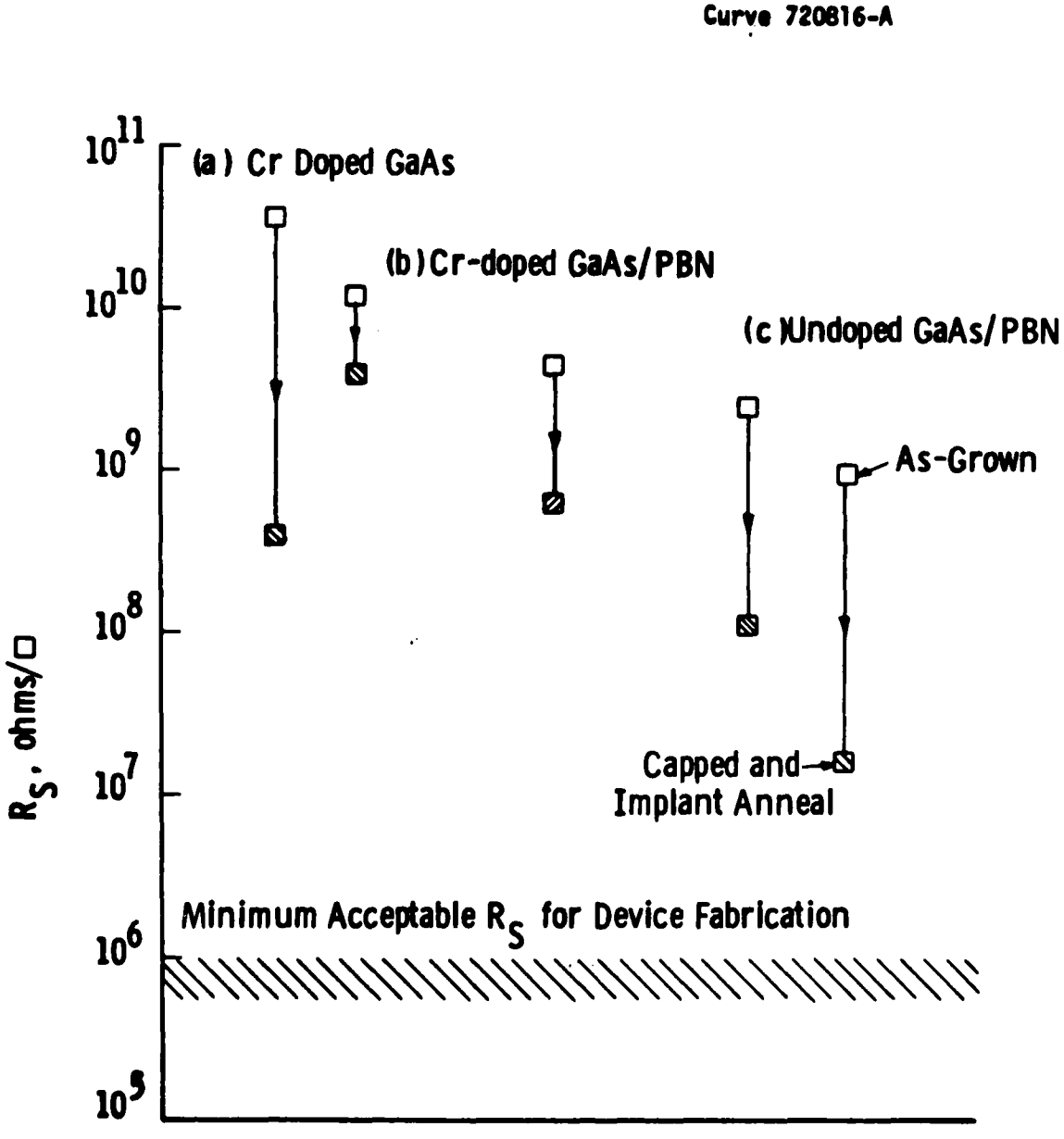


Figure A-8. Thermal Stability of Undoped and Cr-Doped LEC GaAs Substrates After Si_3N_4 Capping and 860°C/15 m Annealing

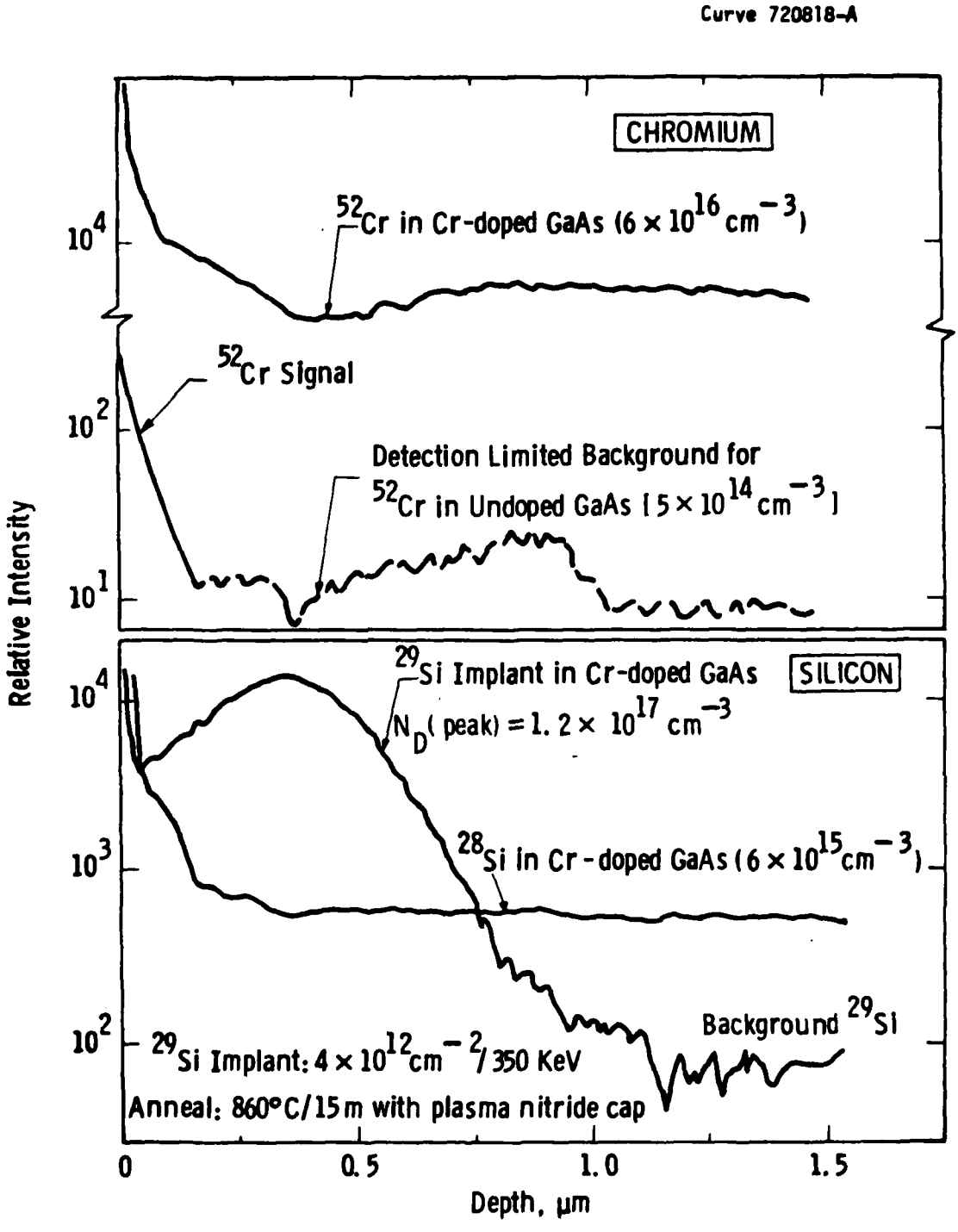


Figure A-9. SIMS Profiles of Silicon and Chromium Distributions in Cr Doped GaAs After ^{29}Si Implant and Annealing. Residual Cr Profile of Implanted GaAs/PBN Sample Is Also Shown.

published results.[1] In contrast to these published data, only slight Cr depletion is observed near the peak of the $^{29}Si^{+}$ implant.

Electrical activity profiles of ^{29}Si implants in semi-insulating GaAs were obtained by C-V measurements using evaporated Al Schottky barrier diodes. Plots of the variation of net donor concentration with depth of implants in undoped GaAs/PBN substrates are shown in figure A-10 and represent the uniformity across each slice and from slice-to-slice in this material in both activation efficiency and profile shape. The data shown was measured on three slices cut from the first half of an undoped GaAs/PBN crystal. The data shows a high degree of uniformity for direct substrate implants and similar uniformity and reproducibility has been achieved for implant energies between 125 and 400 keV. As shown in figure A-10, the measured profiles can be fitted to the tabulated joined half gaussian profile,[19] provided modifications[20] are made to the latter to allow for energy loss in the Si_3N_4 and diffusion. The depth of maximum concentration (R_M) is 2650Å and the deep and shallow standard deviations (σ_d and σ_s) are 1000 and 1400Å respectively.

The profiles shown in figure A-11 are typical of ^{29}Si implants into Cr-doped GaAs substrates. Poor agreement with the theoretical LSS profile is apparent, although SIMS profiling of the ^{29}Si implants in Cr-doped substrates yields approximately gaussian distributions (see figure A-9). The abrupt fall-off of the electrical profiles near the $R_m + \Delta R_m$ depth suggests either Cr accumulation in the region and/or Cr depletion at shallower depths. Achievement of this profile is sensitive to the energy of the channel implant and the dose of any shallow (125 kV) implant employed to increase the electron concentration at the surface. Implantation of ^{29}Si into Cr-doped GaAs has generally been characterized by poorer uniformity of activation and profile shape, particularly in highly Cr-doped substrates which exhibit unpredictable and often anomalous implant profiles.

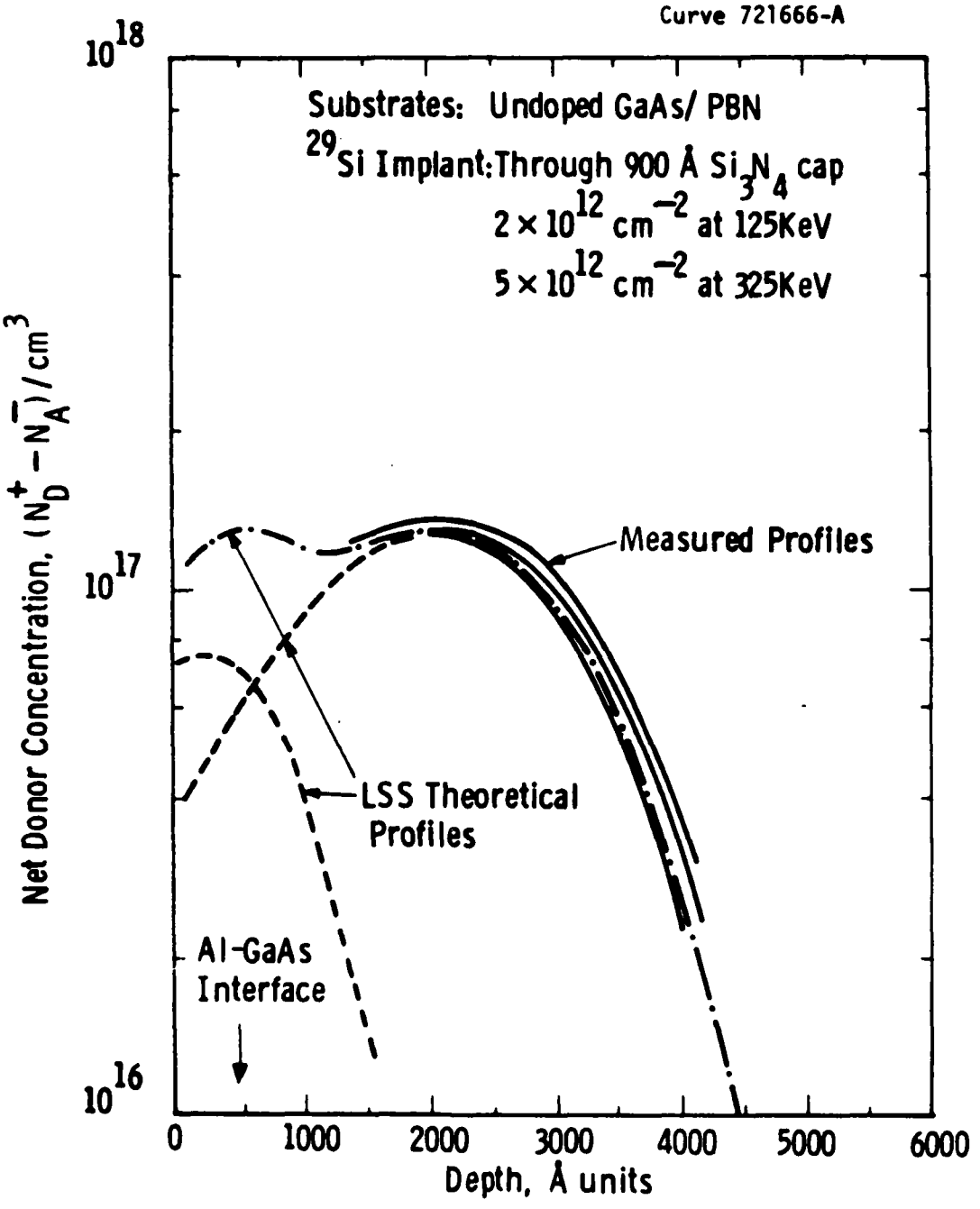


Figure A-10. Uniformity of Implant Profiles in Undoped GaAs/PBN Substrates Measured by C-V Profiling. Implants Performed Through 900Å Thick Si_3N_4 Layer.

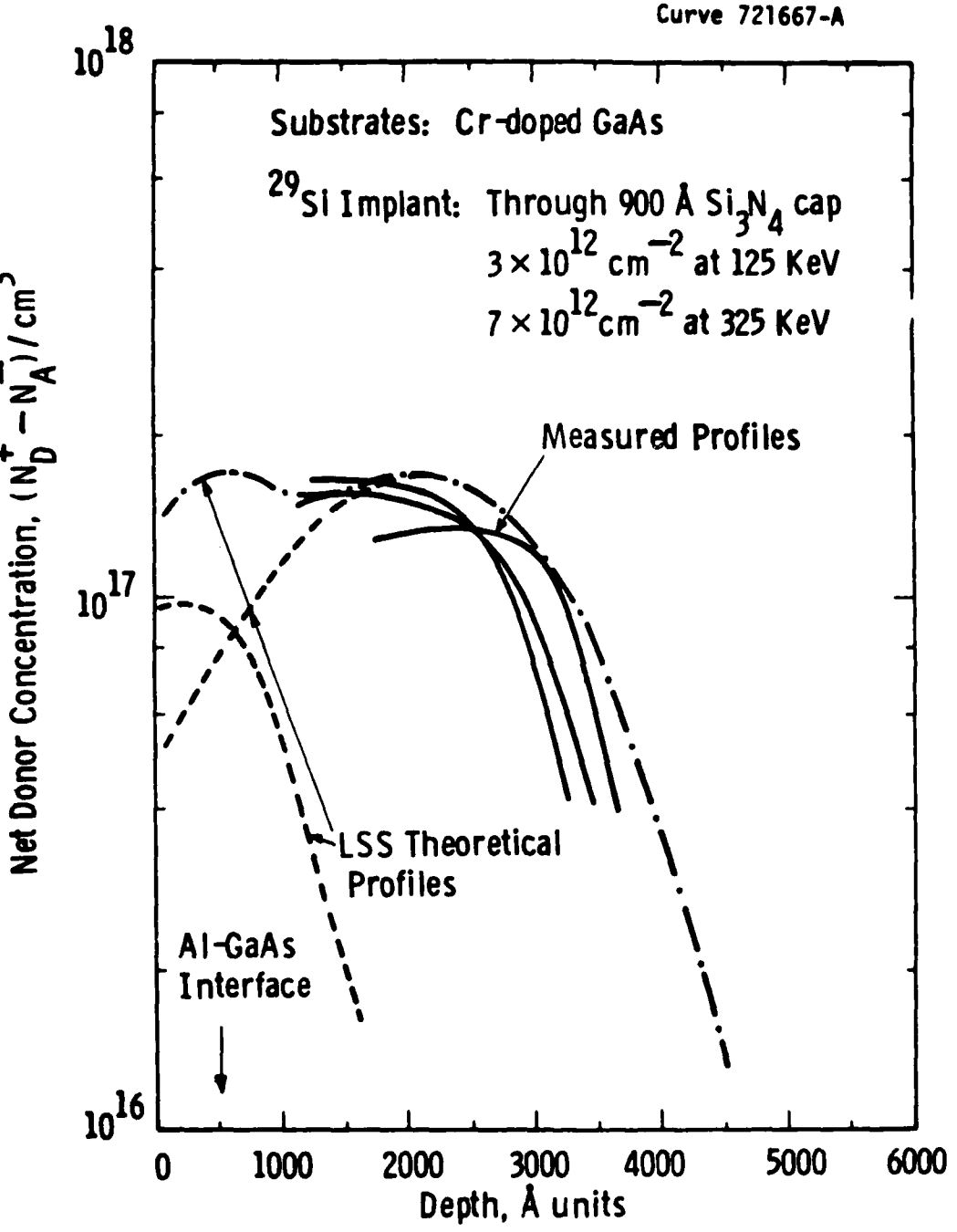


Figure A-11. Implant Profiles in Cr-Doped GaAs Substrates Measured by C-V Profiling. Implants Performed Through 900Å Thick Si_3N_4 Layer.

More detailed measurements of the electrical activation of ^{29}Si implants in semi-insulating GaAs/PBN substrates are shown in figure A-12. Implantations through the Si_3N_4 encapsulant layer at 100, 200 and 400 keV energies were utilized to obtain uniform profiles in this series of experiments. The net donor concentration was obtained directly from C-V measurements and the implanted concentration from the measurement dose and the channel thickness as calculated from the profile data and assumed to be $R_m + \sqrt{\pi/2}\ \sigma_d$. Corrections for surface depletion assuming a 0.6 eV surface barrier and a 40% deposition of the low energy implant in the nitride layer were made. Figure A-12 indicates an activation efficiency of 78%. Similar measurements of other GaAs/PBN substrates indicate that the activation efficiency increases with increasing chromium content [70-80%/undoped; 75-85%/low Cr (8×10^{15} cm^{-3}); 85-100%/high Cr (6×10^{16} cm^{-3}]. The somewhat lower activation efficiencies observed in implanted undoped and lightly Cr-doped GaAs/PBN substrates are consistent with the amphoteric nature of silicon in GaAs, so that the implanted silicon can occupy both the Ga and As sublattices. In contrast, the As sublattice sites are already occupied by chromium in more heavily Cr-doped GaAs, and as a result, the silicon resides almost entirely on Ga sublattice sites. Activation therefore approaches 100%.

Figure A-12 also indicates the existence of a small threshold dose for the onset of electrical activation. This threshold corresponds to an excess acceptor concentration in undoped GaAs/PBN substrates which must be compensated before any net electrical activity is observed. The intercept in figure A-12 indicates the excess acceptor concentration N_A is 0.9×10^{16} cm^{-3}. Implants into high Cr content GaAs substrates indicate an excess acceptor concentration in the (5 to 10) $\times 10^{16}$ cm^{-3} range, increasing from seed-end slices to the tang of these Cr-doped crystals. These results suggest that additional Cr in excess of about 1×10^{16} cm^{-3} concentration in GaAs/PBN substrates serves no useful

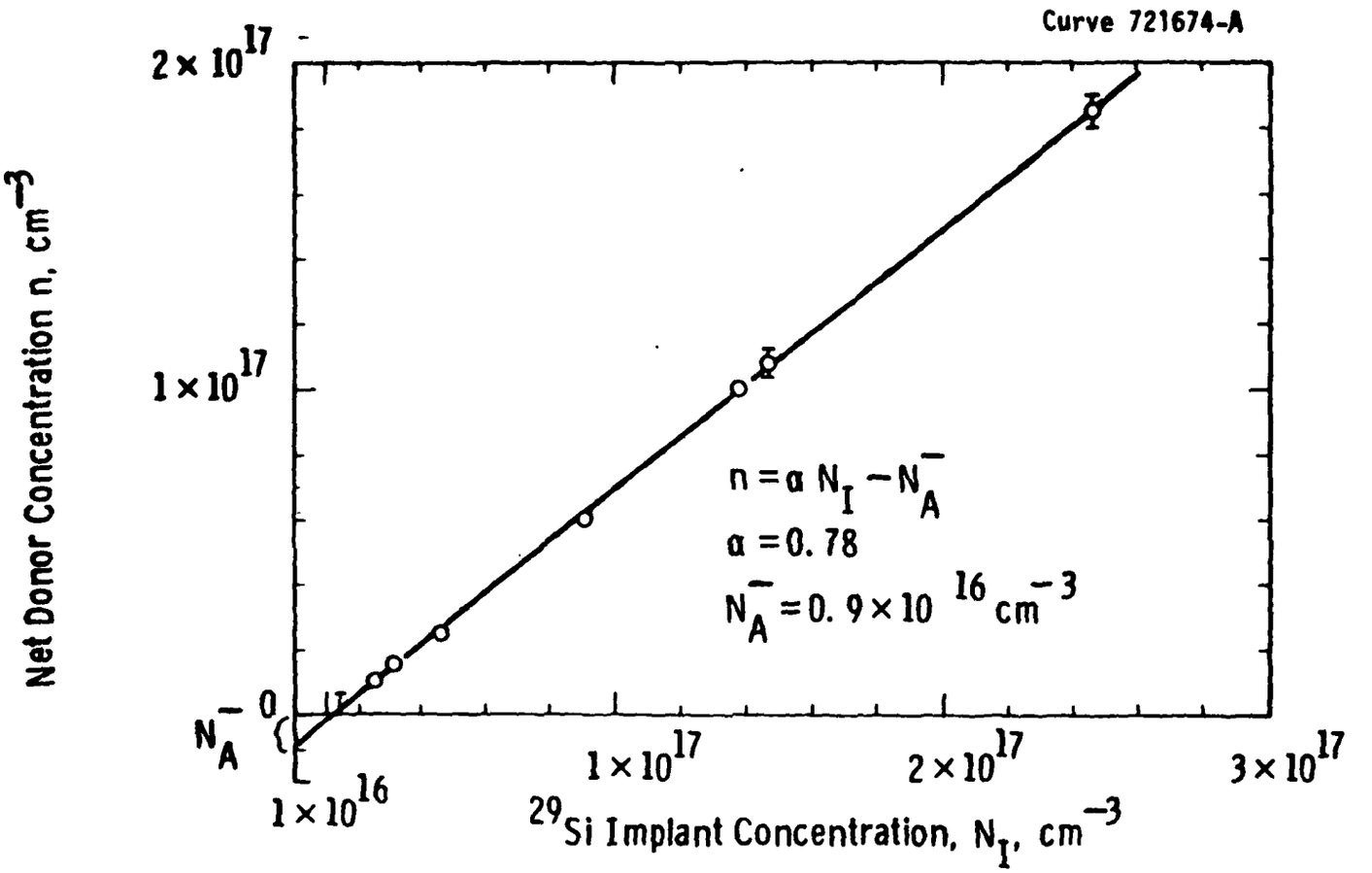


Figure A-12. Activation Efficiency (α) and Substrate Acceptor Concentration (N_A) for ^{29}Si Implants in Undoped GaAs/PBN Substrates.

purpose and contributes to excessive ionized impurity scattering, compensation and redistribution phenomena.

Low-field Hall effect mobilities as a function of the peak donor concentration of direct implanted channels in undoped and Cr-doped GaAs substrates are shown in figure A-13. Data from two undoped GaAs/PBN and three conventional Cr-doped GaAs crystals grown by the LEC technique, as well as Cr-doped boat-grown GaAs, are shown. The implants were performed at energies between 250 and 400 keV, with and without nitride caps and with single and dual energy implants. ^{29}Si implants into semi-insulating GaAs/PBN substrates show the highest mobilities: at peak donor concentrations of about 1×10^{17} cm^{-3}, mobilities of 4,800 to 5,100 cm^2/vsec are measured compared with mobilities in 3,700 to 4,500 cm^2/vsec range for Cr-doped substrates prepared by LEC or boat growth. In lightly doped channel layers (2×10^{16} cm^{-3}), the observed differences are considerably larger - an electron mobility of 5,600 cm^2/vsec in undoped GaAs/PBN substrates versus 3,000 cm^2/vsec in Cr-doped substrates. The measured mobilities of directly implanted channel layers in GaAs/PBN are compared to theoretical bulk mobilities[21] in figure A-13. The higher mobilities observed in undoped GaAs/PBN substrates are consistent with a compensating acceptor density of about 1×10^{16} cm^{-3}, in agreement with the value derived from observations of the threshold dose for the onset of electrical activity (figure A-12).

Mobility measurements were also performed at 77K for the implanted layers in semi-insulating GaAs-PBN substrates. A plot of mobility as a function of peak donor concentration at 77 and 298K is shown in figure A-14. The 77K mobility of 12,000 cm^2/vsec which has been achieved in lightly doped channels (2×10^{16} cm^{-3}) is to our knowledge the highest mobility which has been achieved by direct ion implantation into semi-insulating substrates and is comparable to the mobilities which have been attained in epitaxially grown layers (see, for example, the data compiled by Rosztoczy and Kinoshita).[22]

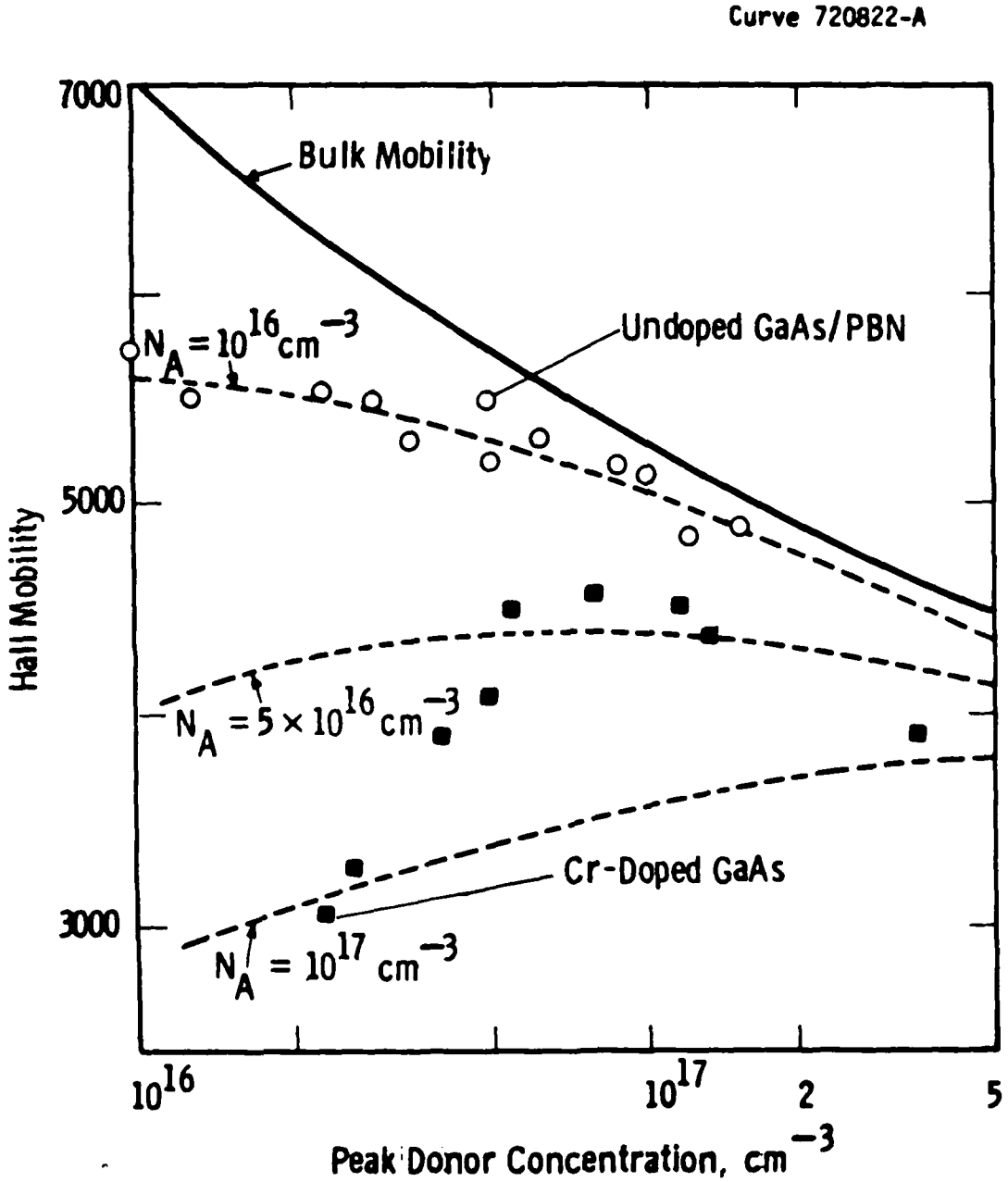


Figure A-13. Measured Direct ^{29}Si Implant Mobility in Semi-Insulating Undoped and Cr Doped GaAs Compared With Theoretical Bulk Mobility

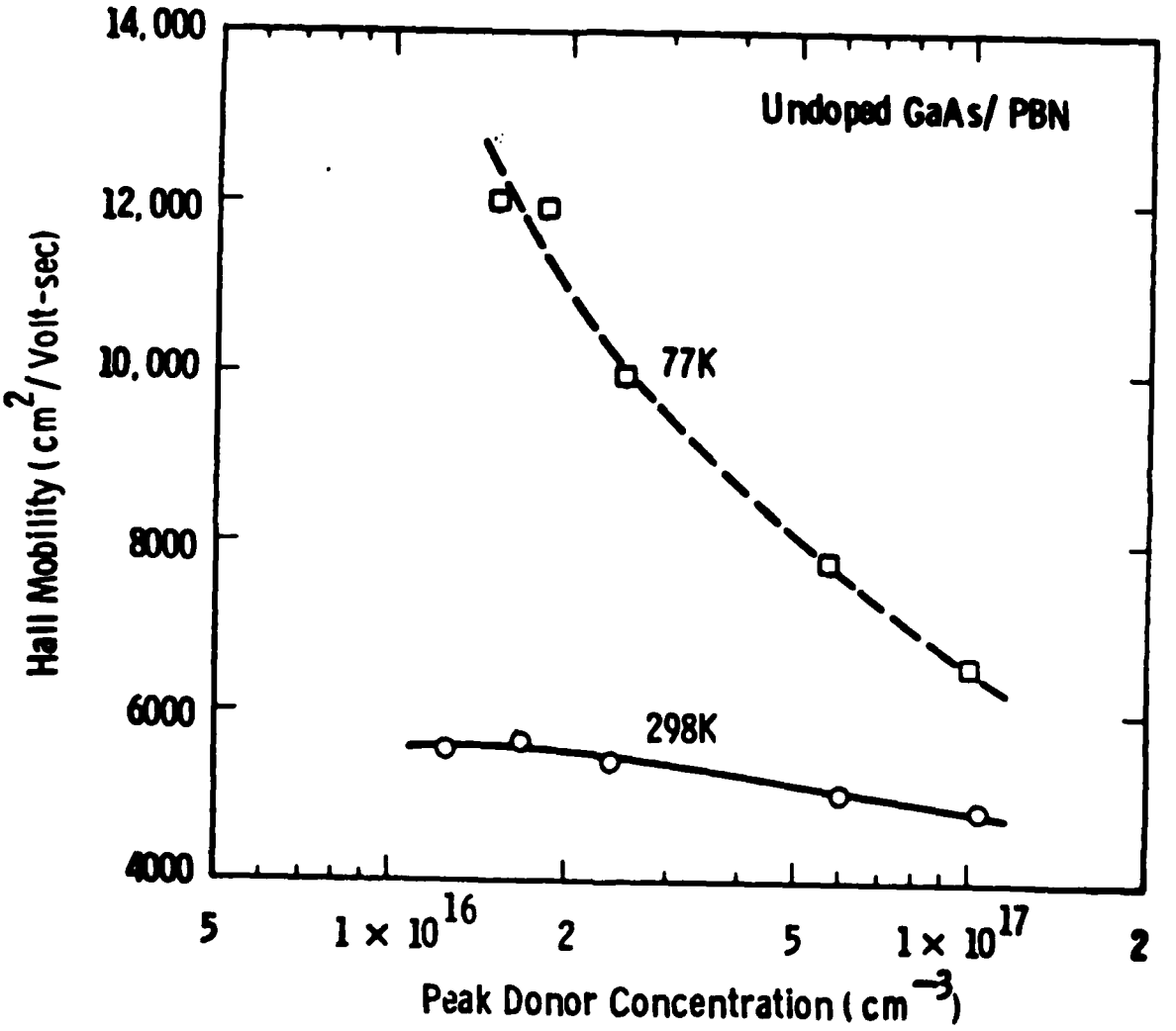


Figure A-14. Measured Mobility at 77 and 298K in Directly Implanted Undoped GaAs/PBN Substrates.

A.5 DISCUSSION AND SUMMARY

The progress made towards developing higher purity, high resistivity GaAs crystals through the use of LEC pulling from pyrolytic boron nitride crucibles is reported in this appendix. The intent is to achieve stable, semi-insulating substrate properties without resorting to intentional doping with chromium (or at least, to reduce the Cr dopant content of GaAs significantly) in order to avoid the serious redistribution problems associated with this impurity at quite low temperatures and their potentially harmful effects on FET device performance and reliability.

It has been shown that large diameter GaAs crystals grown from high purity melts in PBN crucibles contain significantly lower contrations of residual impurities than LFC and boat-grown crystals prepared in fused silica containers. In particular, residual silicon concentrations of (1-2) x 10^{15} cm^{-3} was determined by quantitative SIMS analyses compared to silicon contents of up to 1 x 10^{16} cm^{-3} in other GaAs crystals. High boron and carbon concentrations were, however, observed in GaAs/PBN crystals, but these impurities do not appear to affect the electrical transport properties of ion implanted layers formed in these substrates. Semi-insulating behavior is achieved in undoped GaAs/PBN substrates, although the concentrations of deep acceptor impurities, such as Cr and Fe are at least an order of magnitude less than the Cr doping levels normally encountered in conventional semi-insulating GaAs. The as-grown resistivity and sheet resistance of thermally annealed undoped GaAs/PBN substrates fall in the mid to high 10^7 ohm cm and 10^7 ohm/□ ranges, respectively. Although these resistivities are lower than those of conventional Cr-doped GaAs, acceptably low leakages and RF losses are attained in FET's and analog circuits fabricated on this material. Light Cr doping enables higher resistivities to be attained without adversely affecting the measured electron mobilities in implanted layers.

Direct ion implantation studies of undoped GaAs/PBN substrates using ^{29}Si implants yield highly reproducible implant profiles showing excellent agreement with LSS theoretical predictions. The results suggest a weakly amphoteric behavior of the silicon implants in undoped or lightly Cr-doped GaAs/PBN substrates and demonstrate an excess compensating acceptor concentration of about 1×10^{16} cm^{-3} in these substrates. High channel mobilities of 4,800 to 5,000 cm^2/vsec are obtained in directly implanted channels with (1 to 1.5) $\times 10^{17}$ cm^{-3} peak donor concentrations required for X-band power FET structures.

Excellent power FET performance has been demonstrated from 1 μm gate length devices fabricated on semi-insulating GaAs/PBN substrates in our laboratories.[23] Directly implanted devices exhibit g_m values of about 100 mmho/mm, small signal gains at 8 GHz of over 11 dB and an RF output power of 0.75 watts/mm. A total output power in excess of 1 watt with 5 dB gain at 8 GHz was measured recently from a directly implanted FET device (2,400 μm gate). Preliminary evaluations also indicate that device characteristics of improved uniformity are attained on semi-insulating GaAs/PBN substrates - a significant factor for the design of circuit parameters in monolithic integrated GaAs circuits.

GaAs device fabrication has traditionally been carried out on irregularly-shaped substrates because of the lack of uniformly round substrates in the past. The coracle diameter control[6] is a step in this direction, but is available only for <111> growths and from our limited experience of this method, is found to adversely affect the purity and structural quality of LEC crystals. Figure A-15 illustrates a GaAs boule which has been ground accurately to diameter with an orientation flat. X-ray topographs of test slices reveal that no significant work damage is introduced by the diamond center-grinding operation. The polished slices shown have a diameter of 1.975 ± .001 inch - a thickness of 0.018 inch and a <110> flat. The availability

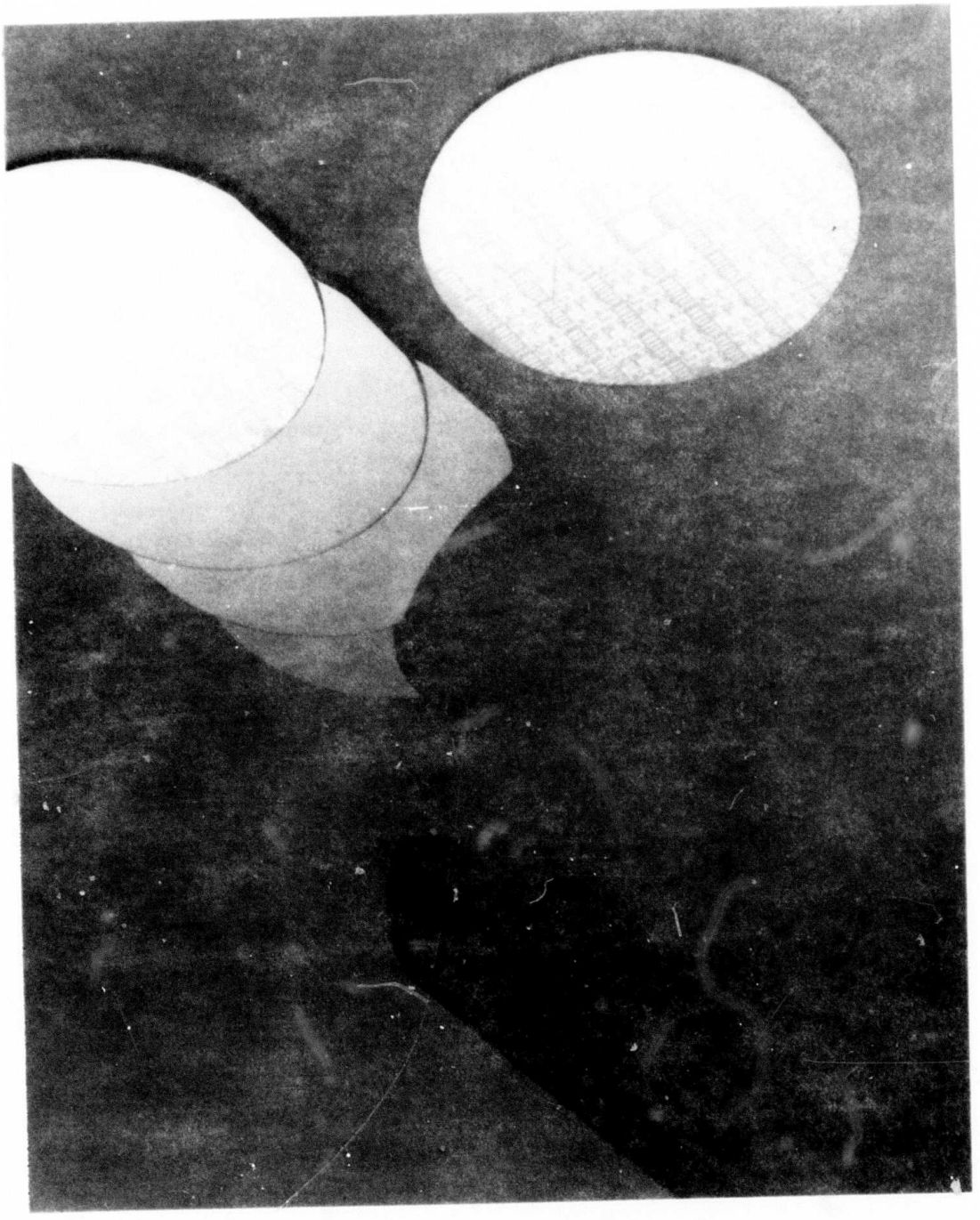


Figure A-15. Center Ground GaAs Boule With <110>
Orientation Flat. Polished Slices Are
1.975 ± 0.001" Diameter and 0.018" Thick

of round oriented <100> substrates fabricated to tight dimensional tolerances with rounded edges (as in silicon technology today) will have important implications as far as moving towards a truly low-cost, higher yield automated GaAs device processing technology in the future.

REFERENCES

1. A.M. Huber, G. Morillot and N.T. Linh, "Chromium Profiles in Semi-Insulating GaAs After Annealing With a Si_3N_4 Encapsulant," Appl. Phys. Latt. 34, 858 (1979).

2. E.M. Swiggard, S.H. Lee and F.W. Von Batchelder, "GaAs Synthesized in Pyrolytic Boron Nitride (PBN)," Inst. Phys. Conf. Ser. No. 336, 23 (1977). See alos R.L. Henry and E.M. Swiggard, "LEC Growth of Inf and GaAs Using PBN Crucibles," Inst. Phys. Conf. Ser. No. 336, 28 (1977).

3. T.R. AuCoin, R.L. Ross, M.J. Wade and R.O. Savage, "Liquid Encapsulated Compounding and Czochralski Growth of Semi-Insulating Gallium Arsenide," Solid State Technology 22 (1), 59 (1979).

4. E.P.A. Metz, R.C. Miller and R. Mazelski, "A Technique for Pulling Crystals of Volatile Materials," J. Appl. Phys. 33, 2016 (1962).

5. J.B. Mullin, R.J. Heritage, C.H. Holliday and B.W. Straughan, "Liquid Encapsulated Pulling at High Pressures," J. Cryst, Growth 34, 281 (1968).

6. Metals Research, Ltd., Melbourn, Royston (Hertz.), England.

7. A. Steinemann and U. Zimmerli, "Dislocation-Free Gallium Arsenide Single Crystals," Proc. Intl. Cryst. Growth Conf. Boston (1966), p. 81.

8. W.C. Dash, "Growth of Silicon Crystals Free of Dislocations," J. Appl. Phys. 28 (8), 882 (1957).

9. J.C. Brice, "An Analysis of Factors Affecting Dislocation Densities in Pulled Crystals of Gallium Arsenide," J. Cryst, Growth 7, 9 (1970).

10. B.C. Grabmaier and J.C. Grabmaier, "Dislocation-Free GaAs by the Liquid Encapsulation Technique," J. Cryst. Growth 13, 635 (1972).

11. P.J. Boksnoer, J.M.P.L. Huybregts, W.M. van de Wiggert and A.J.R. deKock, "Growth of Dislocation-Free Gallium Phosphide Crystals From a Stoichiometric Melt," J. Cryst, Growth 40, 6 (1977).

12. The SIMS Analyses were performed at Charles Evans and Associates, San Mateo, CA using a Cameca 1MS-3f ion microanalyzer.

13. R.K. Willardson and W.P. Allred, Proc. 1966 Intl. Symp. on Gallium Arsenide, Reading, England, p. 35, Adlard and Sons, Ltd., Surrey (1967).

14. Charles Evans, private communication.

15. R.H. Haisty and G.R. Cronin, "A Comparison of Doping Effects of Transition Elements in Gallium Arsenide," Proc. Int. Conf. on Physics of Semiconductors, Paris (1964).

16. R. Zucca, "Electrical Compensation in Semi-Insulating GaAs," Journal of Applied Physics, 48, 1987 (1977).

17. D,C. Look, "On the Characterization of Semi-Insulating GaAs by Hall, Photo-Hall, Photoconductivity and Photomagetoelectric Measurements," J.Elec. Matls. 7,147 (1978).

18. J.G. Oakes, private communication.

19. J.F. Gibbons, W.S. Johnson and S.W. Mylroie Projected Range Statistics, J. Wiley and Sons (1975).

20. The modifications include the assumption that the stopping power of the Si_3N_4 layer is approximately the same as GaAs; the inclusion of third moment estimates in calculating the R_m from tabulated values and the allowance for diffusion broadening according to

$$\sigma^2 = c^2 + 2Dt$$

where $2Dt \approx 3 \times 10^{-11}$ cm^2, with $D = 1.5 \times 10^{-14}$ cm^2/sec

21. W. Walukiewicz, L. Lagowski, L. Jastrzebski, M. Lichtensteiger and H.C. Gatos, "Electron Mobility and Free-Carrier Absorption in GaAs: Determination of the Compensation Ratio," J. Appl. Phys. 50 (2), 899 (1979).

22. E.E. Rosztoczy and J. Kinoshita, "Growth and Evaluation of Epitaxial GaAs for Microwave Devices," J. Electrochem. Soc. 121, 440 (1974).

23. J.G. Oakes, M.C. Driver, R.A. Wickstrom, G.W. Eldridge, S.K. Wang and E.T. Watkins, "Directly-Implanted GaAs Monolithic X-Band RF Amplifiers Utilizing Lumped Element Technology," IEEE GaAs IC Symposium, Lake Tahoe, Nevada, September, 1979.

APPENDIX B

MONOLITHIC MICROWAVE AMPLIFIERS FORMED BY ION IMPLANTATION INTO LEC GALLIUM ARSENIDE SUBSTRATES

B.1 ABSTRACT

A fabrication procedure for broadband monolithic power GaAs integrated circuits has been demonstrated which includes formation of via holes through the 100 μm thick GaAs substrate. A selective implant of ^{29}Si ions into the GaAs substrate is used to dope the FET channel region to 1.2×10^{17} cm^{-3}. The ohmic contacts are AuGe/Ni/Pt and the gates are Ti/Pt/Au. A 1.5 μm thick circuit pattern is achieved using metal rejection assisted by chlorobenzene treatment of AZ1350J photoresist. Using undoped Czochralski wafers of GaAs pulled from a pyrolytic boron nitride crucible, integrated amplifiers have been produced which deliver 28 $\pm$0.7 dBm from 5.7 to 11 GHz. These chips are 2 mm x 4.75 mm x 0.1 mm thick.

B.2 INTRODUCTION

Monolithic power integrated circuits in gallium arsenide offer improved bandwidth over hybrid circuits using discrete gallium arsenide FET's due to the elimination of wire bond inductances. In addition, if the yield of such circuits can be made sufficiently high that the unit cost is low, then phased array radar systems will become economically attractive. Each element of a phased array system may require up to three chips with, for example, power amplifiers, low noise amplifiers and phase shifters. The use of ion implantation directly into semi-insulating substrates containing little or no chromium appears to provide the yield and reproducibility necessary to make these low-cost, monolithic radar components.

We have used selective ion implantation of ^{29}Si into substrates grown in our laboratories to fabricate wideband power monolithic circuits. The selective implantation is truly planar and does not require mesa etching to isolate the active areas of the circuit. The mobility values obtained using unintentionally-doped substrates range from 5700 cm^2/V sec at 1.5×10^{16} cm^{-3} doping to 4700 cm^2/V sec at 1.5×10^{17} cm^{-3}. The uniformity of the carrier profiles is excellent as demonstrated in the paper elsewhere in this issue.[1] The device currents across the GaAs wafer show the same uniformity. In figure B-1 is plotted the source-drain saturation current of the GaAs FET's before the gate is added as a function of the standard deviation of the current. Each data point is the average value for at least five widely spaced points on each wafer. The plot clearly shows that the undoped (chromium concentration $< 5 \times 10^{14}$ cm^{-3}) wafers all have currents whose uniformity is better than the 4% standard deviation, while many of the chromium-doped (chromium concentration $> 2 \times 10^{16}$ cm^{-3}) samples are well beyond the 10% mark.

We have built one-and two-stage monolithic GaAs power amplifiers operating from 5 to 10 GHz using standard photolithographic masking with the addition of a chlorobenzene process[2] to help the metal lift-off. With vias for grounding the sources of the power transistors, these monolithic chips have produced 28 $\pm$0.7 dBm across the 5.7 to 11 GHz band with 6 $\pm$0.7 dB associated gain.

The present paper describes the fabrication details for monolithic power amplifiers and the microwave performance of the resulting chips. The discussion of the fabrication includes information on two methods for achieving via holes. The performance of the passive circuit elements in the microwave matching networks is also considered.

B.3 FABRICATION TECHNOLOGY

B.3.1 Selective Ion Implantation

Wafers are cut from boules grown by the liquid encapsulated Czochralski process. In many cases, these boules are ground to a diameter of 2" with two <110> flats to establish the orientation

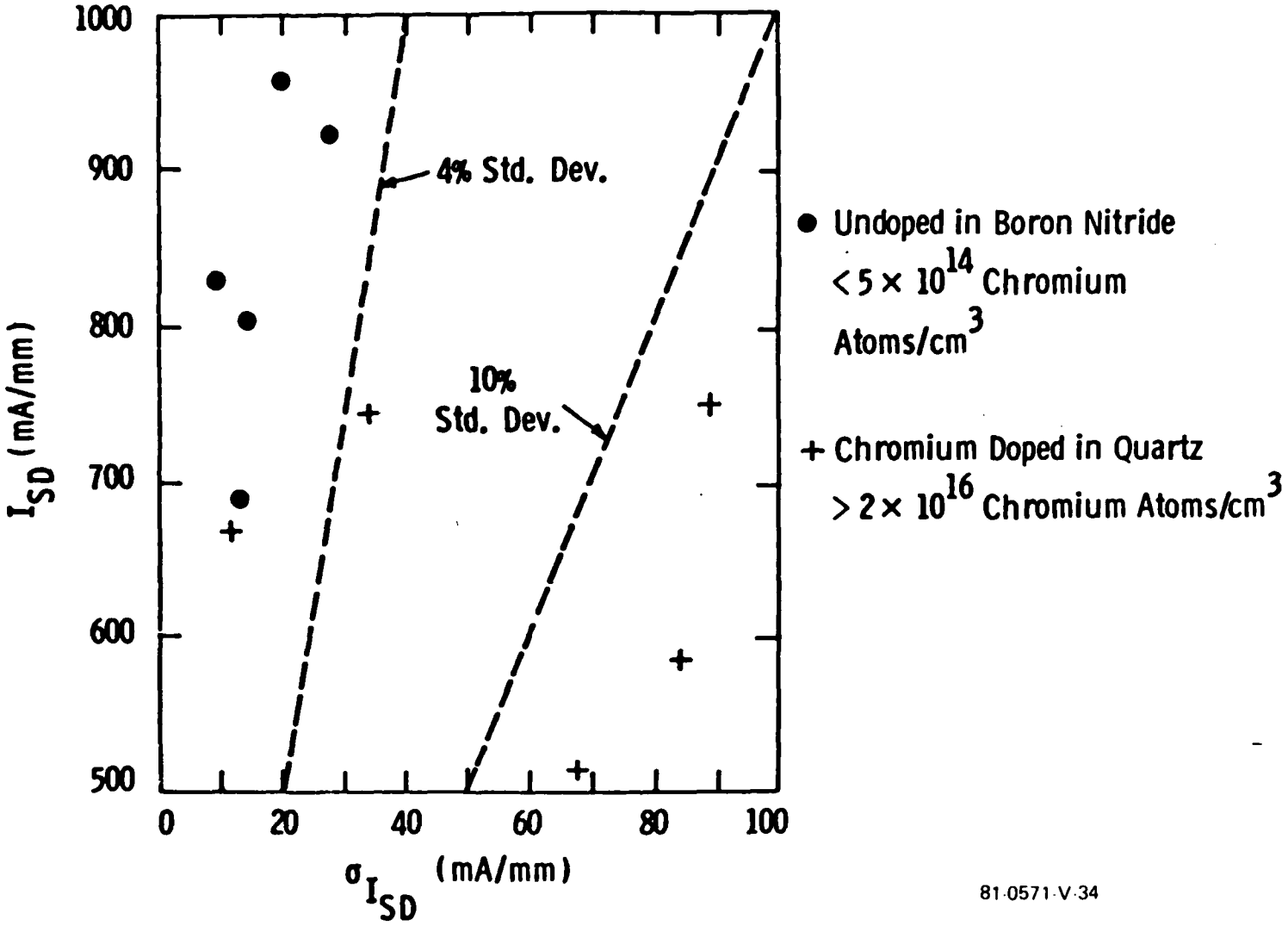


Figure B-1. FET Source-Drain Saturation Current (Without Gate) as a Function of the Standard Deviation of the Current for a Number of FET Fabrication Runs

of the wafers. The wafers are lapped and polished to a thickness of 25 mils before being selectively implanted with silicon (^{29}Si) using the procedure shown in figure B-2. The "front" surface of the gallium arsenide is covered with 1000Å of silicon nitride which is deposited using a plasma-enhanced chemical vapor deposition system which dissociates nitrogen and silane to produce the insulator. 2500Å of 7% phosphorus-doped silicon dioxide (PSG) is deposited on top of the Si_3N_4 using a CVD reactor. A pattern is formed in AZ1350J photoresist and the SiO_2 etched down to the Si_3N_4 to form the ion implantation mask. ^{29}Si ions are implanted through the Si_3N_4 as shown in figure B-2a.

The photoresist is then removed and a second 2500Å thick layer of PSG is deposited as shown in figure B-2b. The phosphorus doping is employed to ensure that this glass becomes plastic at the 860°C annealing temperature and does not lead to stress damage associated with differences in thermal expansion coefficients. The PSG layer is an essential element in the registration of selective implants and prevents pit formation at pinholes in the primary Si_3N_4 encapsulation.

The wafers are annealed in a forming gas (10% hydrogen 90% nitrogen) atmosphere using ramping of the wafer into a furnace such that the wafers rise from room temperature to 860°C in 20 min., their temperature holds at 860°C for 15 min. and then falls back to 25°C in 25 minutes. The furnace contains a flat zone 2-1/2" wide and 8" long.

After the annealing step, alignment marks are formed in the gallium arsenide using ion milling, as shown in figure B-2c, using a further layer of photoresist as a coarse mask. The PSG that was used as part of the first ion implantation mask provides the mask for the area etched into the gallium arsenide surface. This area is, therefore, automatically and precisely aligned with the implanted area.

At the center of each wafer is a square area that is uniformly implanted with ions to provide an evaluation capability for the

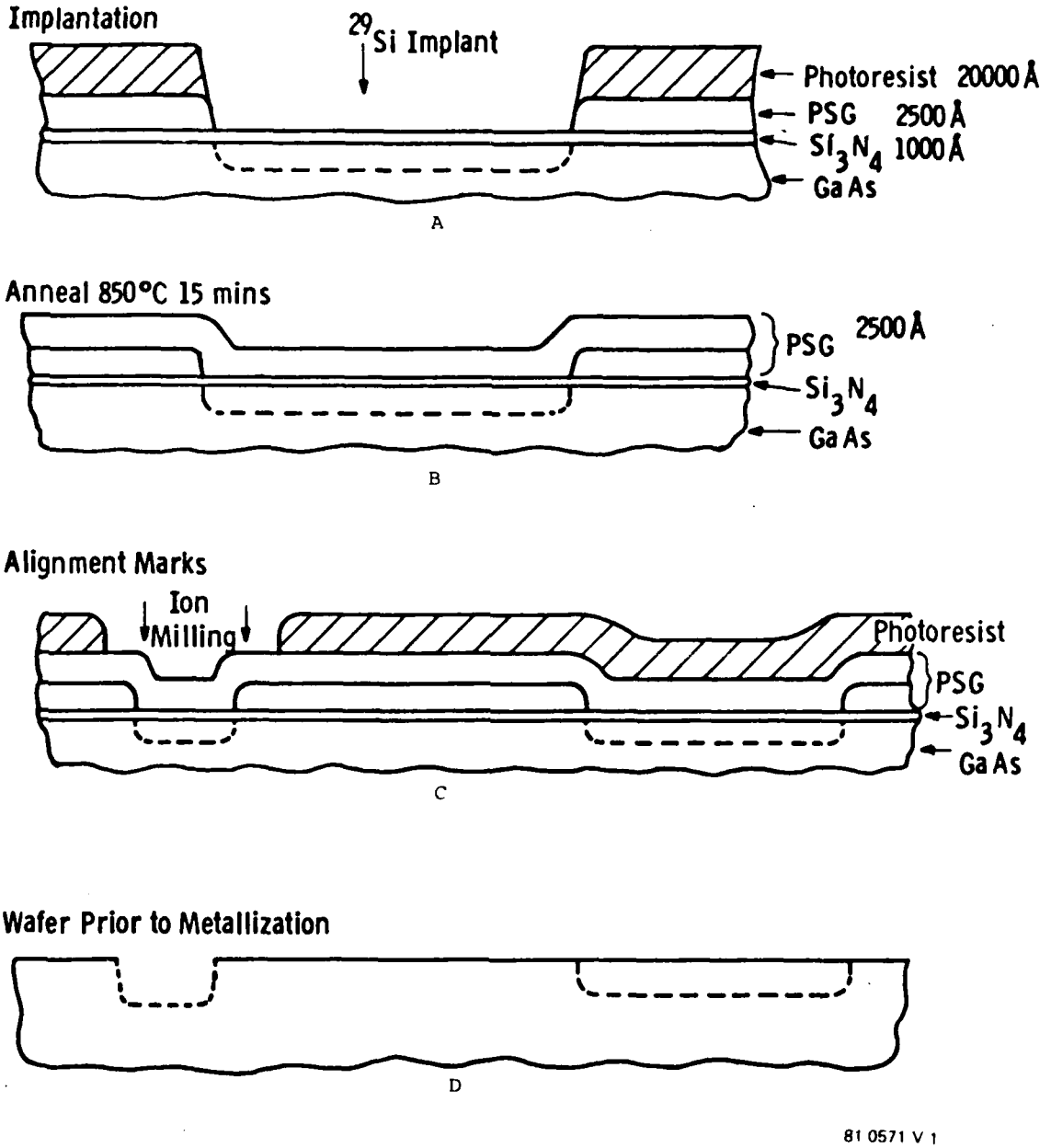


Figure B-2. Schematic Cross Section of Selective Implantation and Alignment Mark Procedures

implant. After the implantation an aluminum dot pattern is formed in this square which allows C-V measurements to be made. It is important at this stage of the device development to know in detail the quality of the implant and activation.

B.3.2 Wafer Metalization

After evaluation, the aluminum dots and the remaining PSG and Si_3N_4 are removed and the wafer is ready for the source-drain ohmic contact metallization which consists of gold-germanium alloy (1200Å) followed by nickel (500Å) and platinum (400Å). When alloyed to a peak temperature of 500°C in forming gas this metal system has consistently produced specific contact resistances less than $3 \times 10^{-6} \Omega\text{-cm}^2$. The metal is defined by a lift-off process using AZ1350J photoresist 1 μm thick. A schematic cross section of the ohmic metallization prior to lift-off is shown in figure B-3a. In order to assist the lift-off process, the photoresist is treated with chlorobenzene in the manner described later in this paper.

After alloying of the source-drain metallization, the gate pattern is defined again using AZ1350 photoresist 1 μm thick as shown in figure B-3b. Prior to deposition of the gate metal the exposed gallium arsenide surface is etched up to 1000Å to form a recess into which the gate is deposited.[3] The metals evaporated are titanium (500Å), platinum (500Å) and gold (4500Å). The gate is offset in our present design being spaced 1.5 μm from the source contact and 3.5 μm from the drain contact in order to minimize the source resistance while maintaining adequate gate-drain spacing to avoid premature breakdown at the drain edge.[4] The metal is again defined by a lift-off process involving chlorobenzene treatment.

The final metallization on the front of the surface of the wafer is the circuit metal which consists of chromium (800Å), palladium (100Å) and gold (14,000Å). This amount of metal is the minimum necessary since at the lowest frequency of interest (5 GHz) the skin depth in gold is 1.1 μm. The ohmic contacts are also partially covered with this thick metal to reduce their spreading resistance (see figure B-3c).

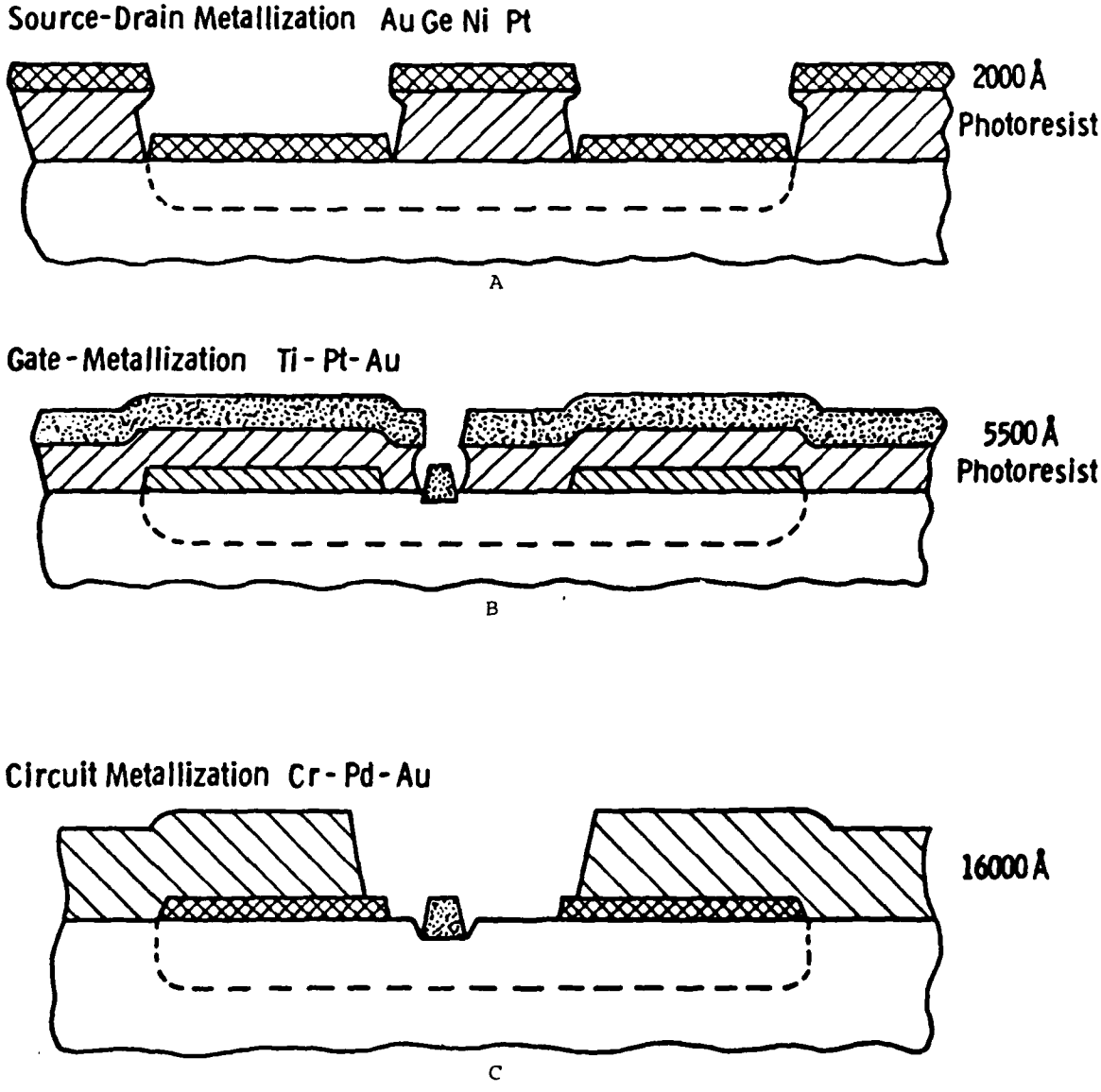


Figure B-3. Schematic Cross Sections of Wafer Metallization Processes

The chlorobenzene treatment[2] mentioned earlier is again used for the photoresist defining the circuit metallization. A schematic diagram of the process is shown in figure B-4. After exposure of the AZ1350J photoresist and before development, the photoresist is soaked for 6 min. in chlorobenzene at room temperature. The action of the chlorobenzene is to form an altered layer on the surface such that after development a lip is formed which causes a break in the metal that is subsequently evaporated. A scanning electron micrograph of a 1 μm long gate opening in 1 μm thick AZ1350J photoresist is shown in figure B-5. Note the 1000Å wide overhang at the upper surface of the photoresist. The GaAs surface has been etched through the opening in the photoresist to form the gate recess.

B.3.3 Via Technology

Vias have been used successfully in discrete FET's[5] to make connections between the source contacts of the FET's and the ground plane on the back of the gallium arsenide wafers. Monolithic amplifiers which rely upon microstrip transmission lines for matching circuitry present a design trade-off between thermal considerations and low loss circuitry.[6] The thickness of the gallium arsenide is chosen to be 100 μm to give acceptable losses in the circuitry, while maintaining satisfactory heat transfer characteristics for the power FET's. With this thickness the problems of fabricating vias are more acute than for the 30 μm thick substrates used in discrete FET's. The via technology is necessary not only to improve the gain of the FET by reducing source inductance but they also provide great flexibility in the circuit design by allowing RF ground to be achieved readily anywhere on the slice. We have developed two different procedures for implementing vias on our monolithic circuits. In the first approach a large area tub (300 μm x 1650 μm) is first etched in the back of the gallium arsenide wafer using AZ1350J photoresist and an acid-hydrogen peroxide-based etch. This tub is aligned to the whole area of the FET on the front of the wafer using infrared techniques. A second AZ1350J photoresist layer is used as an

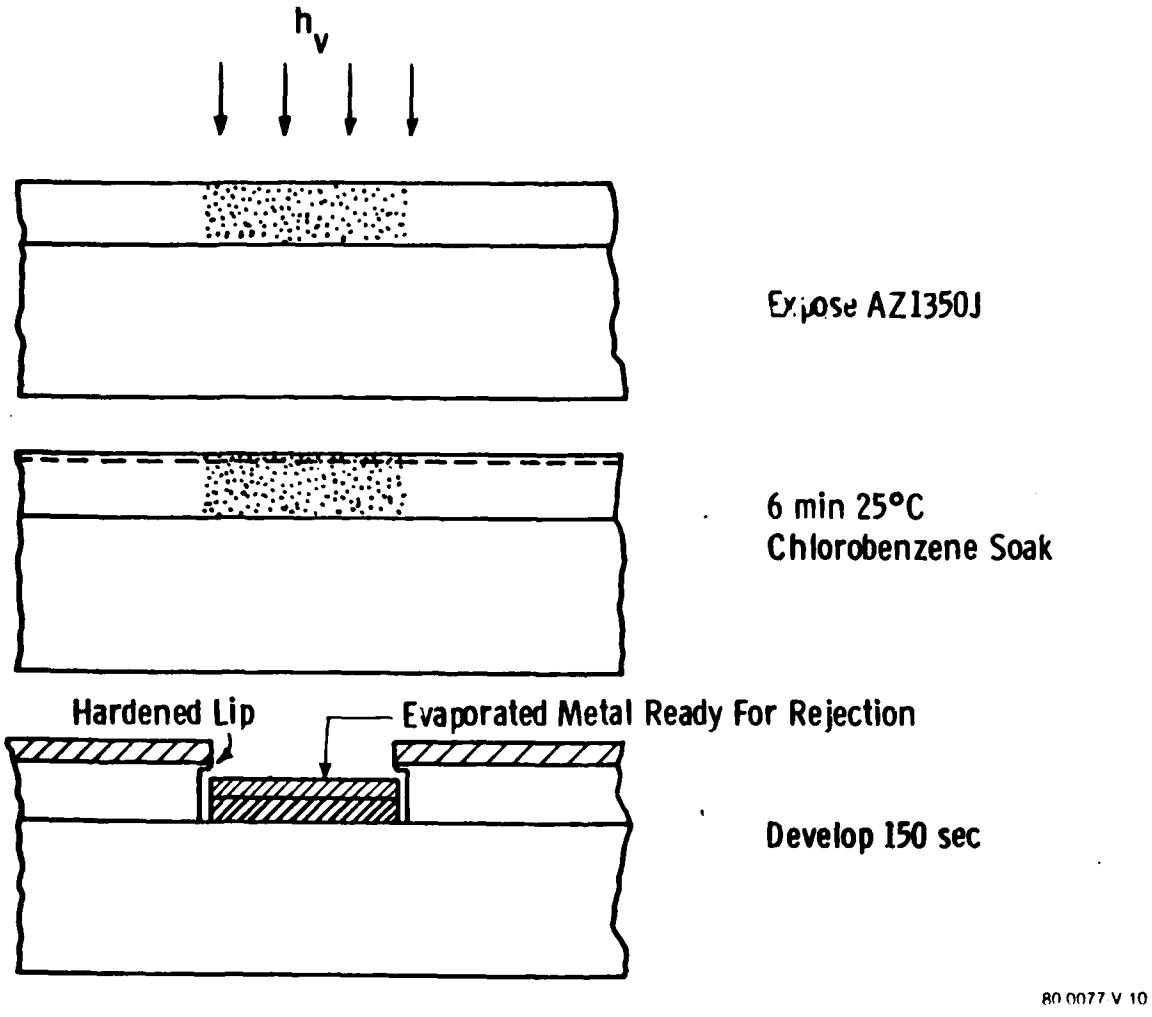


Figure B-4. Schematic Diagram of the Chlorobenzene Treatment of Photoresist

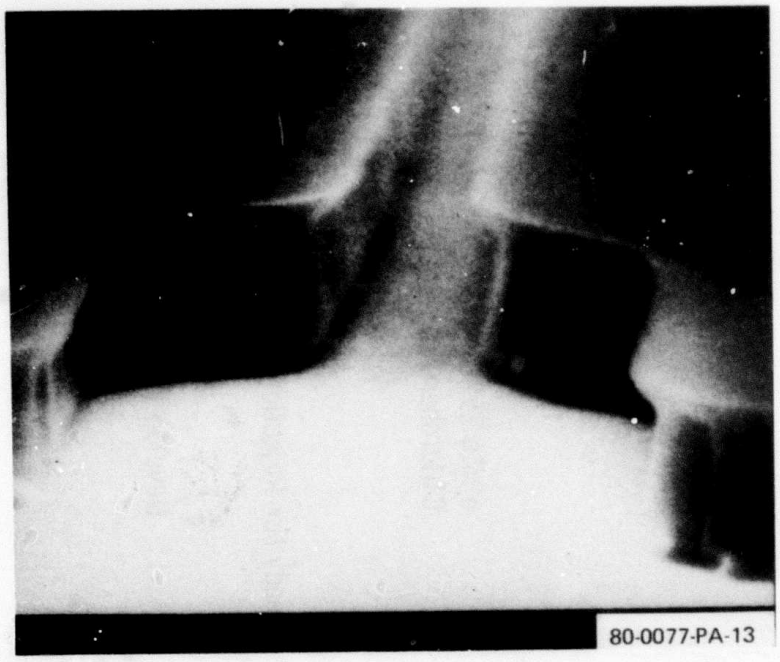


Figure B-5. Scanning Electron Micrograph of 1 μm Gate Opening in 1 μm Thick Chlorobenzene Treated Photoresist

etching mask to produce 100 μm diameter holes to meet each source pad. These holes, together with the back of the wafer, are subsequently metallized with Ti/Au to form the via connections and ground plane, respectively. The etched tubs and vias are shown in figure B-6.

This "complete" via technology has a drawback in that it requires source pads that are 150 μm long (the gate length) by 125 μm wide in order that the etched vias do not destroy the channel regions of the device. Using air bridges or wire bonds to interconnect the sources would require a width of no more than 50 μm which means a 75 μm reduction in FET width for each 300 μm of device periphery and hence a considerable savings in chip area. An additional problem with this technology is that the final etch is designed to be made through a thickness of no more than 25 μm, and hence this process is very sensitive to the uniformity of the wafer thickness.

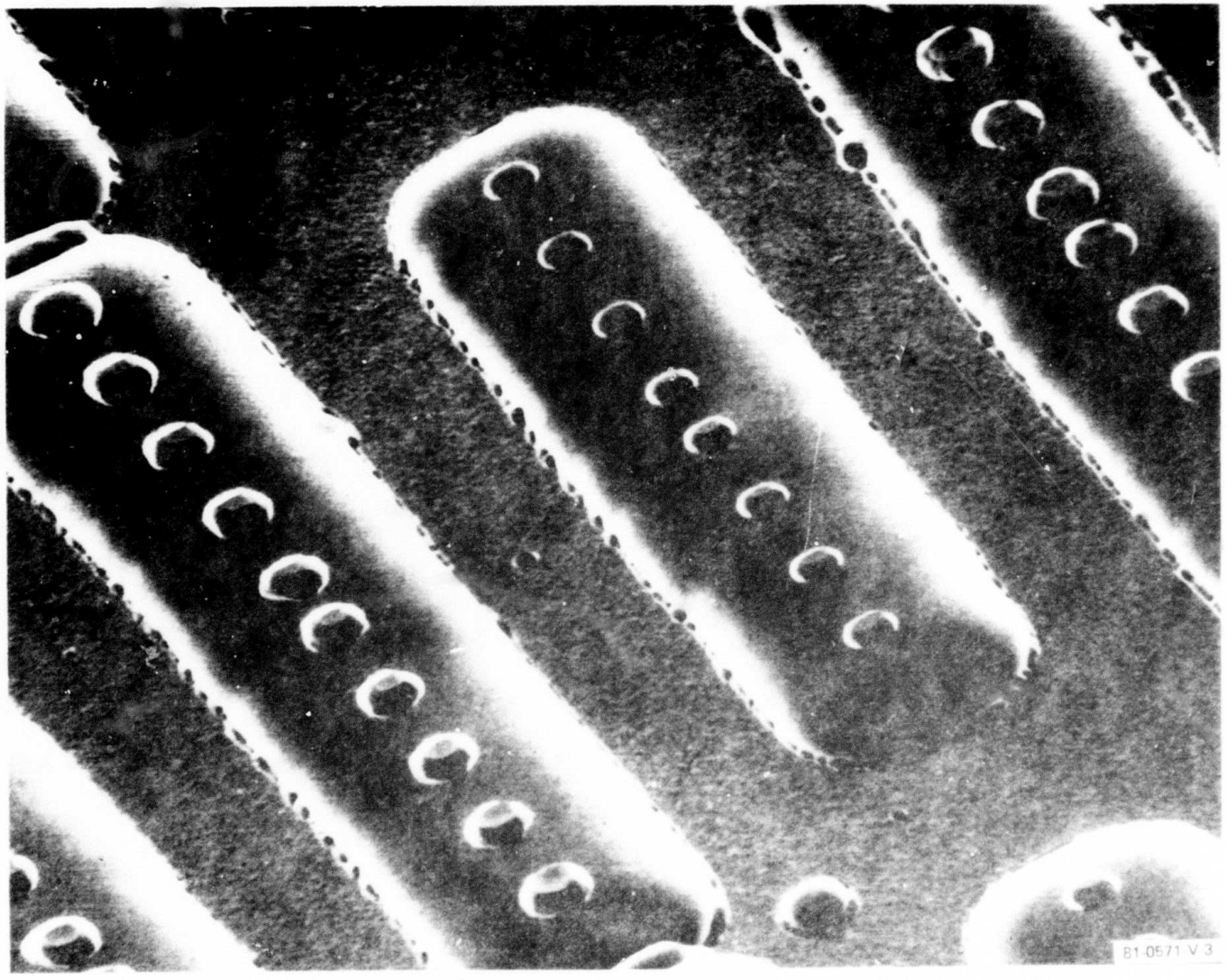


Figure B-6. Scanning Electron Micrograph of Etched Tub and Vias

In the second approach, the circuit is designed with a few large area (250 μm x 250 μm) vias as shown in figure B-7. Vias are located at each end and at the center of the output transistor, at each end of the input transistor, and on two capacitors in the interstage matching network. The sources are interconnected using bond wires. The limited use of vias ("sparse" vias) allows a single etch step on the back side to reach the pads on the front of the slice, hence improving processing simplicity. The yield of vias for this process is better than 99% over the wafer.

B.4 MICROWAVE CIRCUIT CHARACTERISTICS

B.4.1 Passive Elements

The microwave circuits consist of interdigitated capacitors and short microstrip inductors, typically less than 60^{o} electrical length which minimizes the chip area required. The interdigital capacitors are based on a 10 μm center-to-center spacing of the fingers with a 5 μm gap between adjacent pairs as shown in figure B-8. While the length of each finger in a capacitor can be as long as 300 μm, both the length and the number of fingers is varied to produce the desired capacitance with an upper limit of about 1 pF. The photograph shows the clean definition of the capacitor which is necessary for high yield and adequate voltage capability. The application of dc bias voltages across the interdigital capacitors was examined to ensure no degradation in their microwave performance at up to 20V. The data of figure B-9 shows the leakage currents and microwave characteristics at 8 GHz for a typical interdigital capacitor. The capacitor was wire bonded to ground at the end of a 50Ω microstrip line. Application of dc bias was then effected using an external bias tee on an automated network analyzer while measuring the S-parameters from 2 GHz to 12 GHz. At all bias voltages, -20V to +20V, the capacitor and bondwire combination looked like a well-behaved series R-L-C circuit with 1.25 , 0.539 nH and 0.758 pF. This corresponds to a Q at 5 GHz of 33.6 without including any correction for the loss in the 50Ω microstrip line. From the data in figure B-9, the

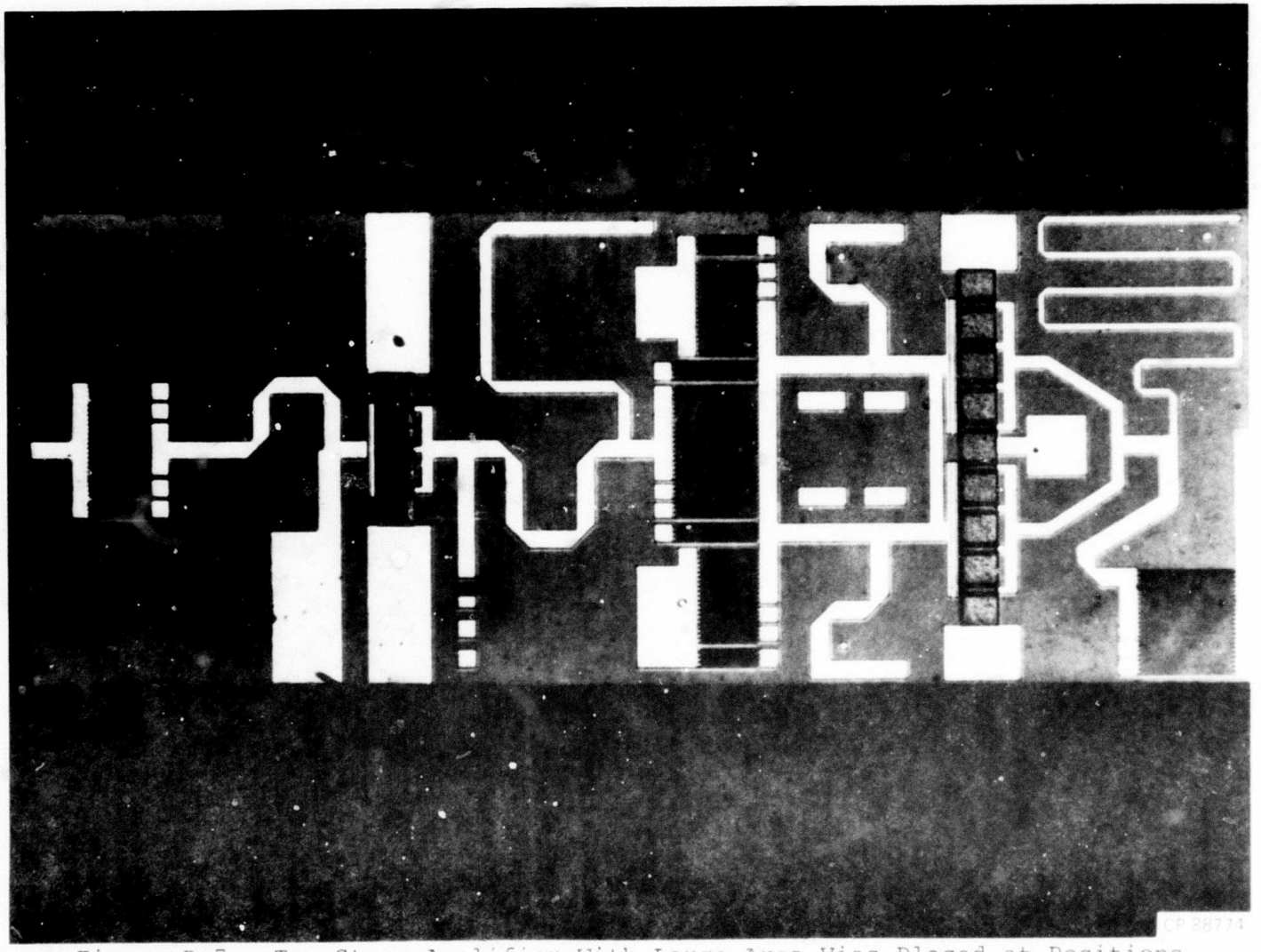


Figure B-7. Two-Stage Amplifier With Large Area Vias Placed at Positions Marked With Circular Dots

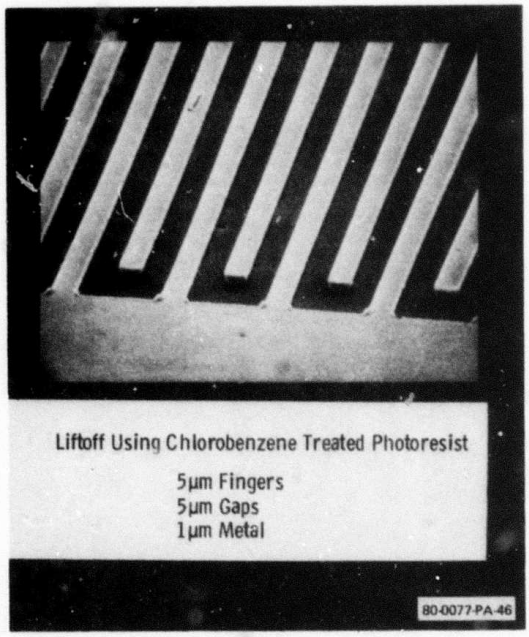


Figure B-8. Interdigital Capacitors Formed on GaAs Using Lift-Off Techniques With Chlorobenzene Treated Photoresist

leakage current of the capacitor up to as much as 20V was 200 μA. This leakage current was independent of the polarity of the applied bias voltage. The phase and magnitude of the reflection coefficient at 8 GHz are nearly unchanged as a function of applied bias, generally staying within 1^{o} of phase and 0.005 in magnitude. We conclude that the interdigital capacitors can be used for form high performance microwave tuning elements capable of blocking up to 20V of dc bias.

The microstrip inductors are typically 50 to 100 μm wide and less than a quarter wavelength long. Since the microstrip transmission line uses a lower ground plane, this form of inductor has been adopted instead of a lumped inductor requiring no adjacent ground plane to simplify the mounting of the finished IC chips and enhance the heat sinking of the active devices on the chip. The chips have several microns of gold with a nickel barrier on the bottom and are soldered to gold-plated copper headers using a

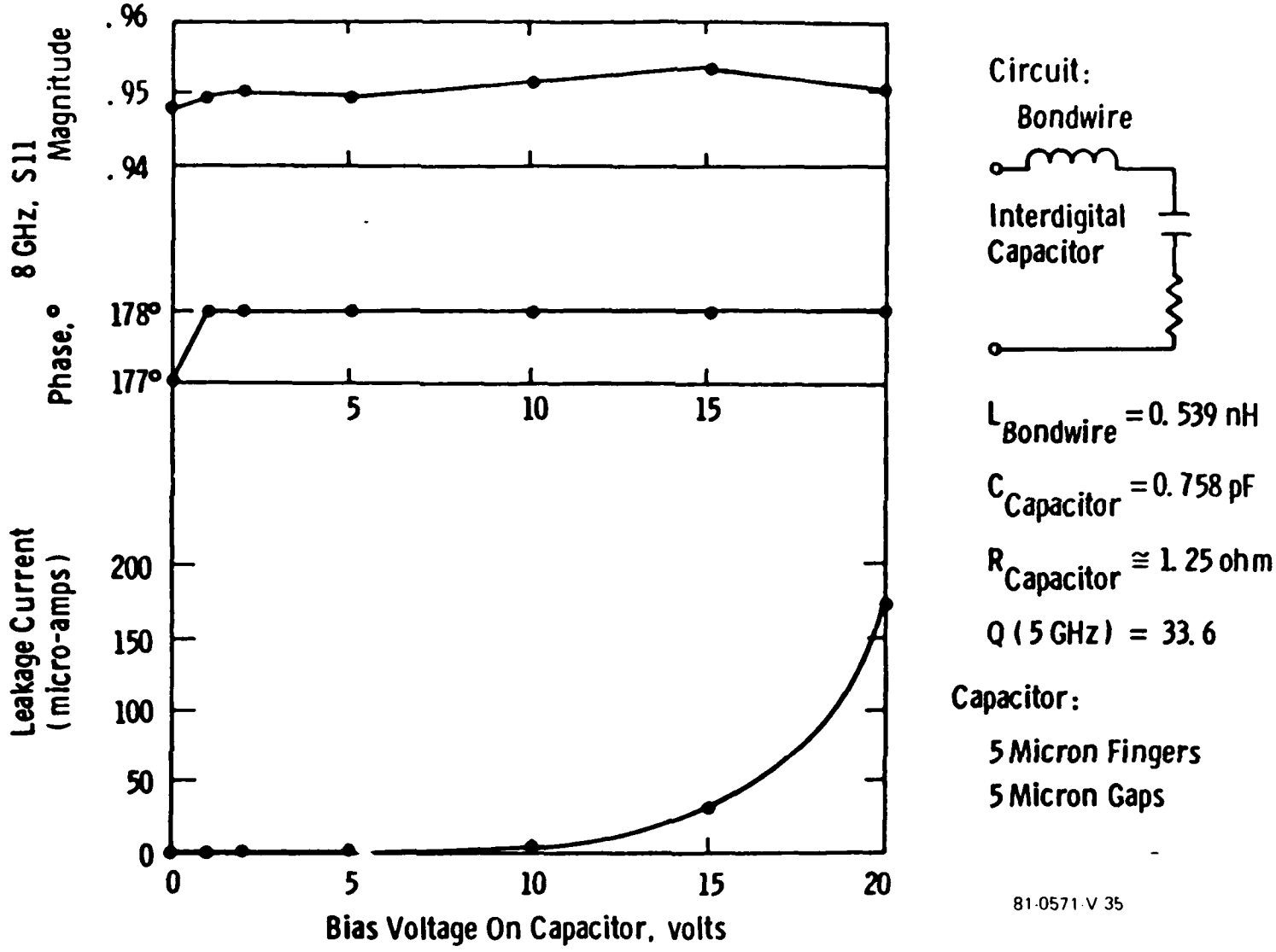


Figure B-9. Effect of Bias Voltage on RF Loss and Leakage Current for Interdigital Capacitors on GaAs

Sn-Au solder at 220°C in a hydrogen atmosphere. The use of a soft solder has reduced chip breakage problems with chips up to 4.75 mm long, while the hydrogen atmosphere enhance the wetting of the solder.

The microwave characteristics of passive circuits using the interdigital capacitors and microstrip inductors are readily predictable. The interstage matching network of a two-stage monolithic amplifier was cut out of the chip using a diamond saw and mounted separately on a microwave header. Wire bonds were used to connect the circuit to 50Ω microstrip lines on either end. The unit was then measured on an automatic network analyzer. The reflection loss of the circuit from 2 GHz to 12 GHz and the configuration of its elements are shown in figure B-10., The circuit consists of seven elements, four inductors and three capacitors, mounted both in series and parallel. The measured reflection loss (dashed curves) show a good match to 50Ω near 6 GHz and higher reflection values elsewhere. This is in excellent agreement with the modeled circuit characteristics (solid curve), except for the location of a small resonance near 3 GHz which can be reconciled with the measured values by changing one element value. The model curve represents the degree of accuracy achieved in producing the desired circuit performance without trimming on a monolithic chip.

The two measured curves represent differences in microwave performance caused by the surface finish of the bottom of the GaAs chip. In general, the lapped bottom surface shows greater deviation from the modeled result than the polished surface case due to higher losses. The lapped surface was produced using 1 μm alumina lapping compound to bring the GaAs wafer to 100 μm thickness. The polished chip came from a wafer which was lapped to 150 μm thickness and further thinned using a bromine:methanol polish solution to 100 μm thickness.

B.4.2 Integrated Circuit Performance

The fabrication of microwave monolithic integrated circuits using selective ion implantation has produced one- and two-stage broadband power amplifiers with up to one watt output power. The

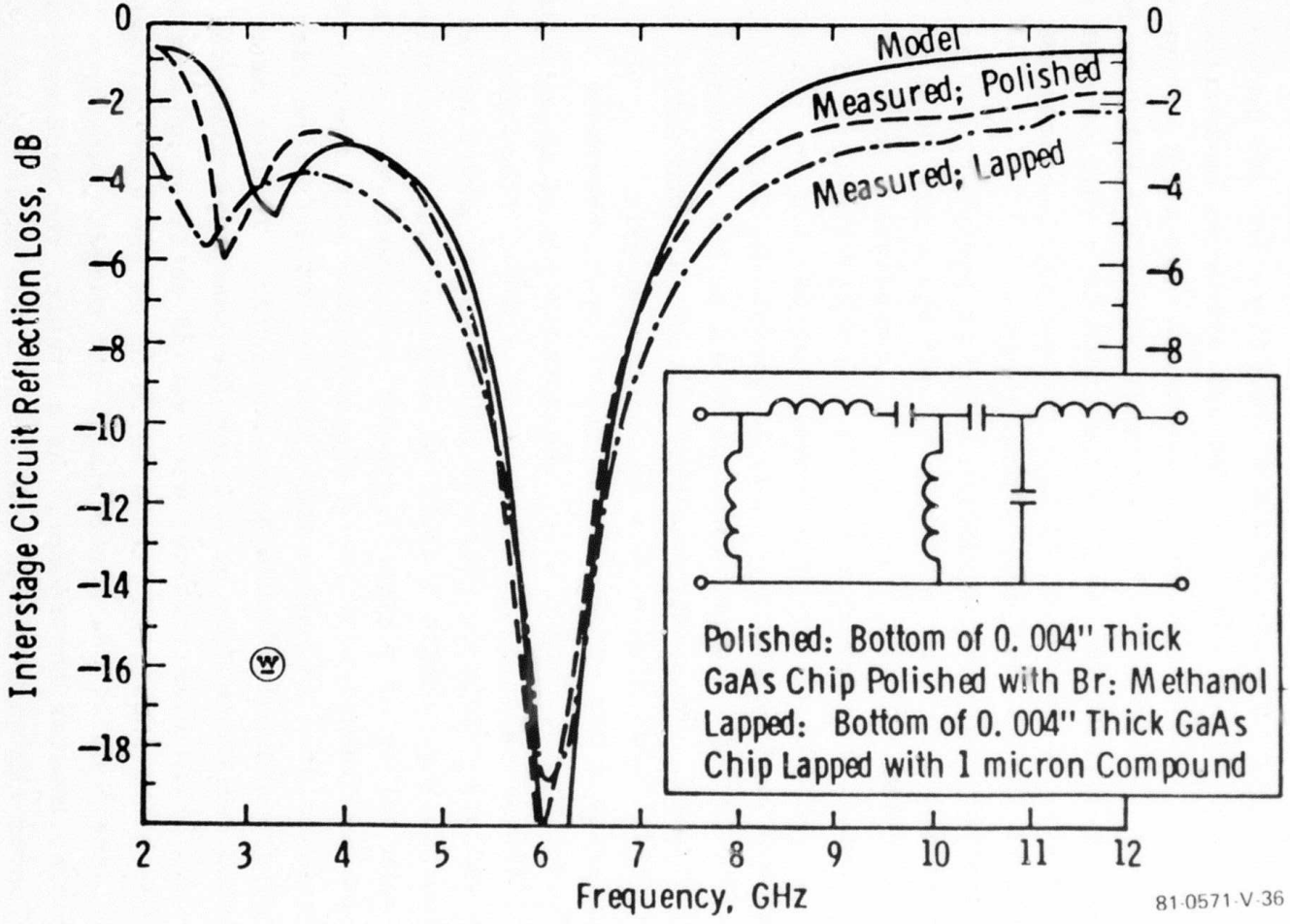


Figure B-10. Predicted and Measured Responses of a GaAs IC 7-Element Interstage Matching Network

discrete power FET's from these runs produce better than 0.5 W/mm at 8 GHz with best results of 0.7 W/mm for a 900 μm periphery FET (0.63W) and 0.66 W/mm for a 2400 μm periphery device (1.6 watts). When incorporated in a single-stage amplifier, the 900 μm periphery FET was matched from 5 GHz to 10 GHz and exhibited better than 5 dB gain over this band at 100 mW output power. The single-stage amplifier is shown in figure B-11. The input and output matching networks use two capacitors and five inductors on a chip of 1.25 mm x 3.375 mm size. Optimization of this circuit has produced 400 mW from 5 GHz to 10 GHz with over 3 dB of gain.

A two-stage amplifier employing a 900 μm periphery FET in the first stage and a 2400 μm periphery second stage was shown in figure B-7. This circuit contains five interdigital capacitors and nine inductors. The chip for the two-stage amplifier is 2 mm x 4.75 mm, but uses a more densely packed circuit. Seven via holes are used on the chip; two to ground the first FET, three for the 2400 μm FET, and two for capacitors in the interstage matching network. This chip has produced 28 $\pm$0.7 dBm output power from 5.7 to 11.0 GHz with 6 $\pm$0.7 dB associated gain.

To understand the effects of RF drive level, frequency and dc bias voltages on the output power characteristics of these broadband amplifiers, three dimensional plots of gain, frequency and output power are generated using an automated microwave power measurement system. While a table of measured data can provide precise gain values at a given frequency and power level, it does not provide an overall picture of the amplifier performance. The characteristics of a two-stage amplifier at two different bias conditions are shown in figure B-12a and B-12b. In each case, the output power capability at a given frequency was monitored as the gate and drain bias voltages were varied until an optimum was found. The plots show gain from 0 to 20 dB on the vertical axis, frequency from 5 to 11 GHz horizontally and output power from 0 to 30 dBm coming towards the reader. As a result, the back wall of the plot shows the gain versus frequency of the amplifier at low

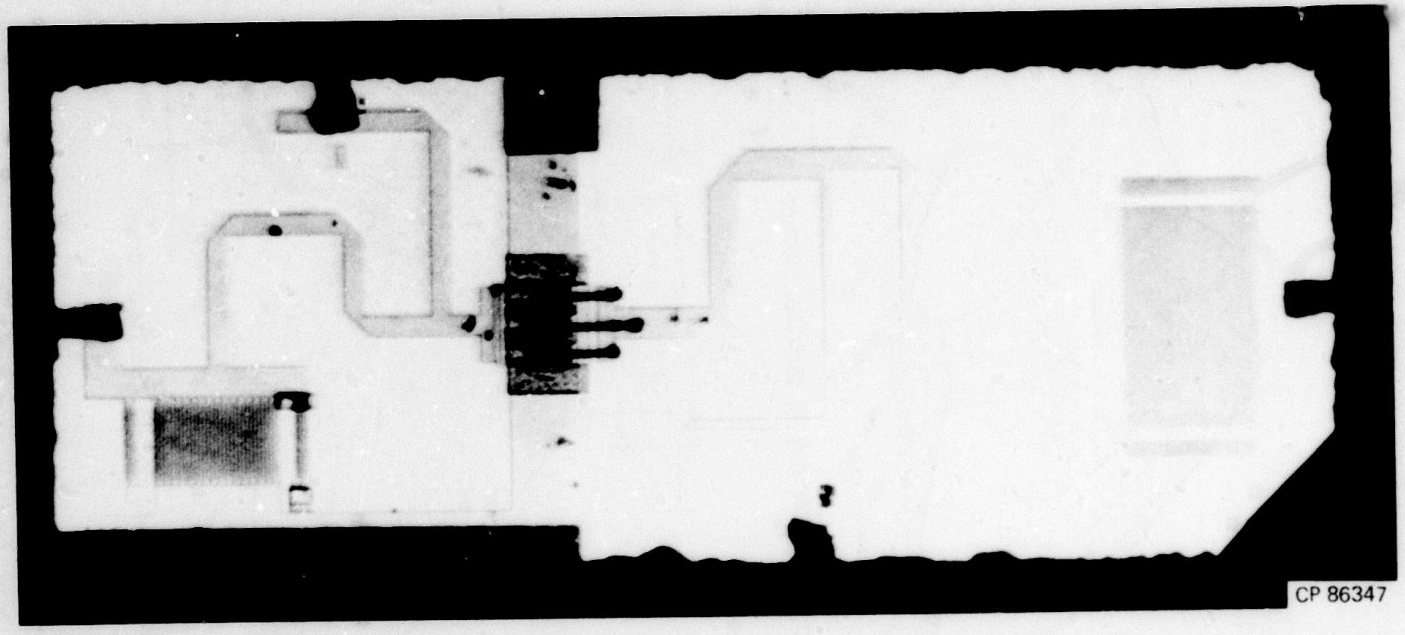
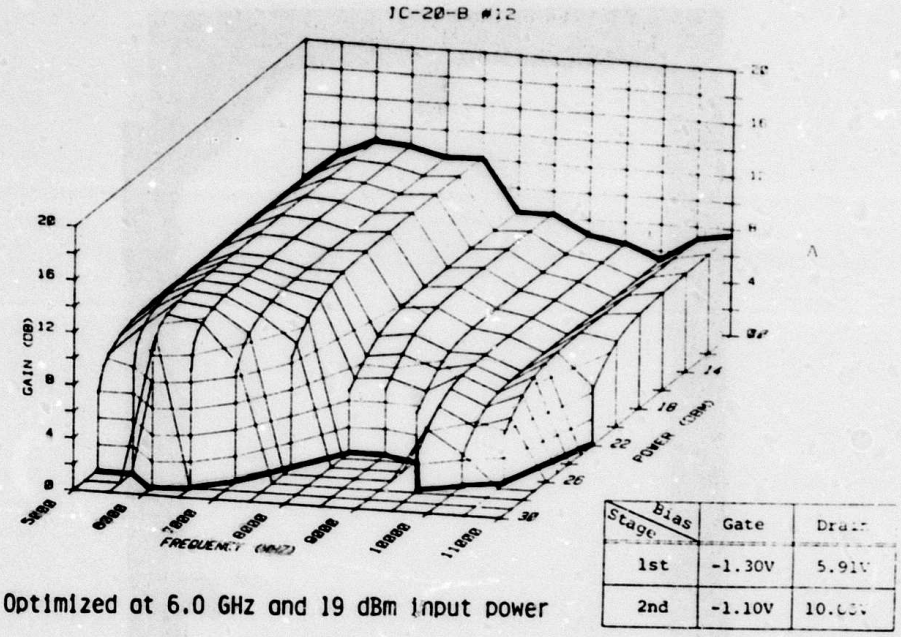
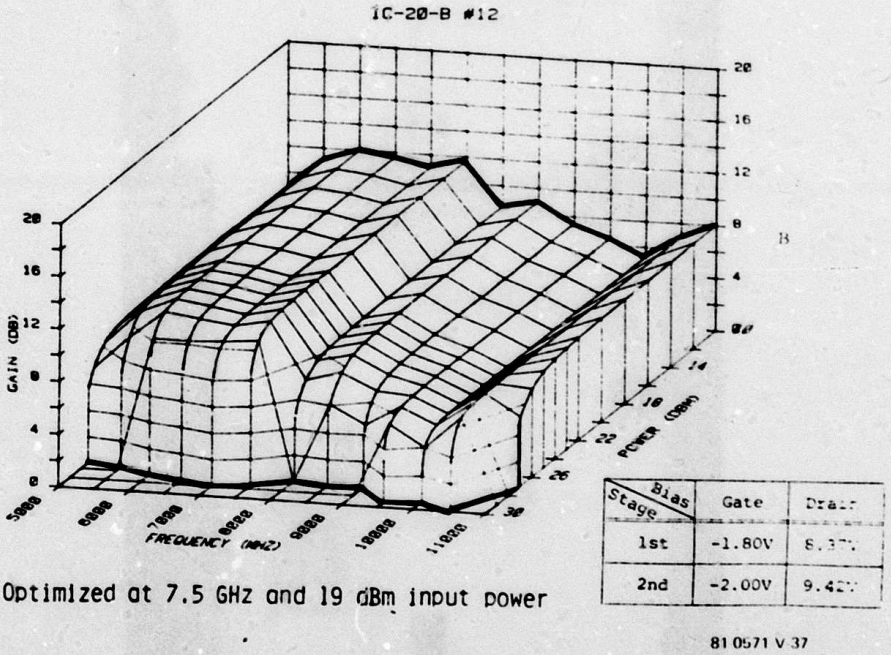


Figure B-11. Single-Stage Octave Bandwidth Amplifier Delivering 100 mW Output Power With 5 dB Gain from 5 to 10 GHz



Stage \ Bias	Gate	Drain
1st	-1.30V	5.91V
2nd	-1.10V	10.03V

Optimized at 6.0 GHz and 19 dBm input power



Stage \ Bias	Gate	Drain
1st	-1.80V	8.37V
2nd	-2.00V	9.42V

Optimized at 7.5 GHz and 19 dBm input power

81 0571 V 37

Figure B-12. Three Dimensional Plots of Power vs. Frequency vs. Gain for a Two-Stage GaAs Amplifier With Transistor Biases Adjusted for Maximum Power Gain at Two Different Frequencies

drive levels or the small signal gain. The front edge near the frequency axis at 0 dB gain shows saturated output power as a function of frequency. From the saturated output power, one can climb the wall to find the output power and gain at any frequency. The curves in figure B-12a, for example, show the amplifier when biased to obtain maximum power at 6 GHz. Notice the high gain from 5.5 to 7.5 GHz with a peak output power or over 29 dBm at 6 GHz with over 10 dB of associated gain. From 8 to 11 GHz, however, not only is the gain lower but the output power does not reach 28 dBm and falls below 25 dBm at 8.5 GHz. By biasing the gates of both FET's closer to cut-off, the input capacitance is decreased and the response shifts up in frequency close to the designed band of 7 to 10 GHz for this amplifier. This is shown in figure B-12b where the output power was optimized for 7.5 GHz using the FET bias conditions. While the small signal gain is only changed by about 1 dB, the saturated output power from 7 to 10.5 GHz never falls below 28 dBm and peaks at 1 watt at 10.5 GHz. The bias point of both FET's for this case was nearly identical and very close to the design values. Further attempts to raise the performance at higher frequencies by bias adjustment proved unrewarding.

The complete RF characterization of the broadband GaAs monolithic amplifiers is a very complicated task. In addition to the usual small-signal tests on a network analyzer, the automated power system provides rapid measurement and display of data over a wide frequency and power range. We expect advanced, automated microwave measurement systems to become increasingly necessary as the complexity of linear microwave integrated circuit chips increases.

B.5 CONCLUSION

Broadband power amplifiers have been successfully fabricated as monolithic integrated circuits on semi-insulating GaAs without added chromium pulled from pyrolytic boron nitride crucibles. Using selective ion implantation of silicon ions directly into the GaAs substrate, power FET's delivering up to 0.7 W/mm at 8 GHz

have been produced. The uniformity of the FET drain-source current has less than 4 percent standard deviation across undoped semi-insulating substrates compared with more than 10 percent for chromium-doped wafers.

A via technology has been used to provide low inductance RF grounding, both for the source electrode of the FET's and selected microwave circuit elements. The vias are etched through the 100 μm thick GaAs substrate to a 250 μm by 250 μm metal square on the top surface of the wafer. The yield of etched via holes across the wafer is better than 99 percent and is unaffected by up to a 25 μm thickness variation across the slice due to lapping and polishing tolerances. This technology improves the gain of the microwave transistors by reducing the source inductance. In addition, the layout of the microwave circuitry is eased by having ground available anywhere on the chip.

The use of 1.5 μm thick evaporated metal films patterned with a photoresist lift-off process allows inductive lengths of microstrip line and interdigital capacitors to be fabricated on the GaAs chip. The resulting amplifiers have produced up to 400 mW from 5 GHz to 10 GHz from a single-stage amplifier and 28 $\pm$0.7 dBm from 5.7 GHz to 11 GHz from the two-stage amplifier.

Further technology improvements will include incorporation of the dc bias circuits on the GaAs chip and the use of air bridges on the power PET's for source interconnection.

B.5 ACKNOWLEDGEMENTS

The authors would like to acknowledge the expert contributions of J. Degenford, D. Boire, R. Freitag and R. Choshtagore of Westinghouse ATL, Baltimore, the technical skills of J. Kotvas, J. Clancy, R. Nye, S. Maystrovich, P. Kost, D. Dustafson, R. McKee of the Westinghouse R&D Center, and the help and encouragement of M. Cohn and H.C. Nathanson. This program is partially funded by the Defense Advanced Research Projects Agency through the Office of Naval Research and the Naval Research Laboratories under Contract N00014-78-C-0268.

B.7 REFERENCES

1. H.M. Hobgood, G.W. Eldridge, D.L. Barrett and R.N. Thomas, "High Purity Semi-Insulating GaAs Material for Monolithic Microwave Integrated Circuits," IEEE Trans. Electron Devices, this issue.
2. B.J. Canavello, M. Hatzakis and J.M. Shaw, "Process for Obtaining Undercutting of a Photoresist to Facilitate Liftoff," IBM Tech. Disclosure Bull., Vol. 19, No. 10, 1977.
3. S. Tiwari, L.F. Eastman and L. Rathbun, "Physical and Materials Limitations on Burnout Voltage of GaAs Power MESFET's," IEEE Trans. Electron Devices, Vol. ED-27, pp. 1045-1054, 1980.
4. R. Yamamoto, A. Higashisaka and F. Hasegawa, "Light Emission and Burnout Characteristics of GaAs Power MESFET's," IEEE Trans. Electron Devices, Vol. ED-25, pp. 567-573, 1978.
5. L.A. D'Asaro, J.V. DiLorenzo and H. Fukui, "Improved Performance of GaAs Microwave Field-Effect Transistors with Via Connections through the Substrate," in IEDM, Dig. Papers, pp. 370-371, 1977.
6. R.A. Pucel, "Some Design Considerations for Gallium Arsenide Monolithic Circuits," Proceedings Seventh Biannual Cornell Elec. Eng. Conf., pp. 17-32, 1979.

APPENDIX C

FABRICATION CONSIDERATIONS FOR MULTISTAGE MONOLITHIC POWER INTEGRATED CIRCUITS

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Recent improvements in the purity of large two and three inch diameter GaAs substrates, coupled with direct selective ion implantation producing 5000 $cm^2/v\text{-}s$ mobility at 10^{17} cm^{-3} doping, have made broadband linear integrated circuits very attractive. Our two stage power amplifiers have demonstrated 10.8 dB gain from 5 GHz to 9 GHz and broadband output powers of up to .80 watts. To optimize the RF performance of linear power IC's requires the involvement of device engineers in the microwave design process, an area traditionally divorced from device design considerations.

Three areas will be used to illustrate the influence of the device engineer on the performance of a two stage amplifier. The first consideration is the reproducibility of the doping level of the FET channel and an estimate of the expected variations in the power transistors as the channel characteristics are varied. This analysis shows the sensitivity of one, two and three stage amplifiers to doping variations and establishes working limits for specifying the starting wafer tolerances.

A second area is the method chosen for source grounding of the FET's. Conventional wire bonding, plated-through "via" holes and a combination of vias for each 1200 micron cell with wire bonding between sources have all been used. Microwave modelling has shown a significant increase in the parasitic capacitances of large power FET's using vias to ground each source which, while it does not reduce the maximum available gain, does change the optimum matching impedance. The IC fabrication and performance of all three source grounding schemes will be discussed along with their matching problems.

Finally, we will relate the thinning of the GaAs wafer to RF loss in the microwave circuitry on the IC chip. The thickness of the semi-insulating GaAs substrate is a compromise between the higher loss of the microwave matching networks on thin substrates and the need for a low thermal impedance. We have chosen 100 microns thickness for our designs and keep the RF loss low by polishing the back surface of the wafer before metallization. A comparison of microwave circuit loss in a seven element passive circuit on 100 micron thick GaAs has shown about 0.5 dB improvement when using a polished back over that obtained by lapping with 1 micron abrasive. This result is consistent with the observation that the 1 micron (40 microinch) roughness of the lapped surface is nearly equal to the skin depth at 5 GHz in gold.

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*This work was supported in part by the Defense Advanced Research Projects Agency through the Office of Naval Research and the Naval Research Laboratories under Contract N00014-78C-0268.

APPENDIX D

DIRECTLY IMPLANTED GaAs MONOLITHIC X-BAND RF AMPLIFIER UTILIZING LUMPED ELEMENT TECHNOLOGY*

A monolithic GaAs amplifier containing four lumped inductors and two interdigital capacitors has been fabricated with over 20-percent yield on a 1.25 x 2.5-mm chip using direct-ion implantation. The overall amplifier exhibits a one-stage gain of 6 dB centered at 7.1 GHz with a 10-percent bandwidth. No post-fabrication adjustment on any tuning element was required to achieve design goals. One key to the potential of this largechip "monolithic" technolgy is the fact that the per-area yield of the passive circuitry (L's, C's) is generally 50 to 100 times as great as the yield-limiting mechanisms in the active channel of the power FET's. As a result, adding passive circuitry to the FET chain in a controlled lithographically-defined manner only decreases the number of chips per wafer, rather than geometrically reducing the chip yield.

In order to establish a GaAs integrated-circuit technology to eventually reduce the cost of multistage X-band power amplifiers below $100/amplifier, we have been studying the uniformity and reproducibility of direct-ion implantation utilizing a 400-kV Varian Extrion Ion implanter, Model 400-10. We are presently utilizing 6-to 18-cm^2 GaAs substrates which are implanted at 400 keV with 3-5x10^{12} cm^{-2} dose utilizing Si^+ as a dopant. Post-implantation capping is carried out in a modified LFE plasma nitride despoition system at 341°C and the wafer annealed for 15 min at 860°C in forming gas.

In the device process, a 900-μm gate FET having a 1-micron gate and a 6-micron S-D spacing is fabricated utilizing AuGe/Pd/Au ohmic contacts. The input and output matching circuits contain four lumped inductors ranging from 0.15 nH to 1.25 nH plus two 1 pF interdigital capacitors. The circuit metals are over 1 micron

thick to minimize circuit losses. As can be seen in the photograph, figure D-1, the overall size of the one-stage amplifier is only about 3 mm^2, leading us to believe that lumped, high-Q X-band circuit elements can offer substantial size-reduction potential over distributed circuits of the same bandwidth.

The lumped-element circuit design for this amplifier was performed at the Westinghouse Advanced Technology Labs in Baltimore by Mr. D. Maki.

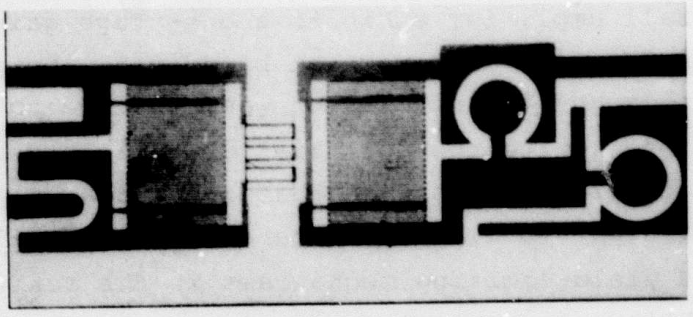

Figure D-1. Ten Percent Bandwidth Monolithic Amplifer

*This work was supported in part by the Defense Advanced Research Projects Agency, through the Office of Naval Research under Contract N00014-78-C-0268.

APPENDIX E

PROCESSING TOLERANCE AND TRIM CONSIDERATIONS IN MONOLITHIC FET AMPLIFIERS

SESSION X: MICROWAVE CIRCUITS

THAM 10.2: Processing Tolerance and Trim Considerations in Monolithic FET Amplifiers

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Westinghouse Electric Corp.

Baltimore, MD

DIRECT ION IMPLANTATION (eliminating the need for buffer layer growth and qualification) offers many advantages for monolithic amplifiers including lower cost and potentially higher yield and reproducibility. Microwave FETs using direct Si implants into Cr doped semi-insulating substrates have yielded typical power outputs between 0.52W/mm and 0.62W/mm at 8GHz as shown in Figure 1. These devices have been incorporated in single-stage monolithic lumped element amplifiers[1] (Figure 2) to yield 6dB gain over 10% bandwidth at 7.5GHz, Figure 3. These amplifiers have also yielded 350-400mW power out with 3.9dB associated gain (900μ FET). The measured input and output match exhibited by these amplifiers as shown in Figure 3 has confirmed the circuit design procedures used.

For these preliminary single-stage amplifiers, both coplanar and microstrip amplifier designs have been studied. Interdigitated capacitors with 5μ gaps and 5μ fingers are used for all tuning applications where capacitance values $<$ 2pF are required. Typical Q values of 40-50 are measured at 8GHz for metalization thickness 2μ. Lumped inductors are used in the coplanar geometry, while short sections of high impedance transmission lines are used in the microstrip geometry. Measurements to date at low power levels show both designs to be comparable; however, as power levels increase and heat sinking becomes more important, microstrip designs are preferred because of their better heat dissipation capability.

The desirability of fabricating monolithic amplifiers which require no trimming is self evident. However, it is likely to be many years before process variations can be made sufficiently small to achieve high yields and hence low cost for applications requiring large sets of multistage amplifiers which must be gain and phase matched over a large frequency range. During the evolutionary period, the ability to trim monolithic ICs will be an invaluable aid which can be built into the design.

To investigate the practicality of trimming techniques, a two-stage 1W amplifier with 10dB associated gain was designed as shown in Figure 4. The design was optimized for 10dB associated gain (Figure 5) over the 5-10GHz frequency range. Analysis of processing tolerances established that the most common process variations were channel doping density (± 20%) which results in a ≈ ± 10% change in input (gate-source) and output (drain-source) capacitance, and gate length variations (± 20%) which result in a corresponding ± 20% change in input capacitance and ± 20% change in the input gate resistance. An extensive analysis has been performed to study the effect of these variations and ways of trimming to compensate for these variations. As an example, consider the case for gate length variations of ± 10% and ± 20%.

[1] Oakes, J.G., et al., "Directly Implanted GaAs Monolithic X-Band RF Amplifier Utilizing Lumped Element Technology", *GaAs IC Symposium Digest*, Sept. 27-28, 1979.

The predicted gain response for these cases is shown in Figure 5 along with the nominal value. For the +10% case note the drop at 10GHz to ≈8.5dB. Figure 6 illustrates the effects of 3 ways of retuning the amplifier to compensate for this gate length change. Table 1 compares the values of the twelve circuit elements for the nominal two stage amplifier and the reoptimized amplifier.

By adjusting only four of the most sensitive parameters (L_1, L_5, L_6 and C_2) performance almost as good as a 12-element reoptimization can be obtained. Further, performance obtained by retuning only L_5 and L_6 is almost as good as adjusting four parameters. Hence, amplifier tuning to compensate for a +10% change in gate length can be accomplished with as few as two elements, with no practical necessity for tuning more than four elements.

Calculated gain and transmission phase results have been obtained for −10% and +20% gate length variations and ± 20% channel doping variations.

Acknowledgment

This work was supported in part by the Defense Advanced Research Projects Agency, through the Office of Naval Research and the Naval Research Laboratory under contract N0O014-78-C-0268.

	Element Values For Nominal Design (nH, pF)	*% Change in Element Values Reoptimized For +10% Gate Length Change*		
		12 Element	*4 Element*	*2 Element*
L_1	1.40	12.9(%)	5.7(%)	
L_2	0.59	−1.7		
L_3	0.94	14.9		
L_4	1.10	8.2		
L_5	0.59	16.2	10.2	8.5
L_6	0.45	−13.3	−8.9	−4.4
L_7	0.23	− 4.3		
L_8	0.72	0.0		
L_9	0.42	− 2.4		
C_1	0.21	0.0		
C_2	1.23	18.7	8.9	
C_3	0.46	− 2.2		
C_B	1.00	0.0		

TABLE 1

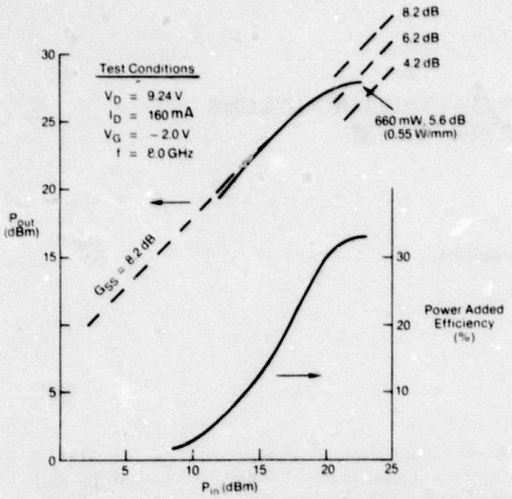

FIGURE 1–P_{out} vs P_{in} for 1200μ directly implanted FET.

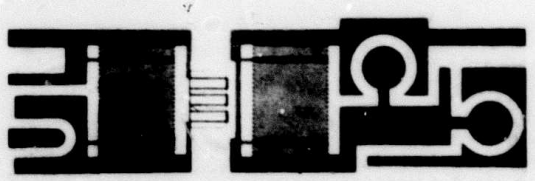

FIGURE 2–Single stage monolithic amplifier.

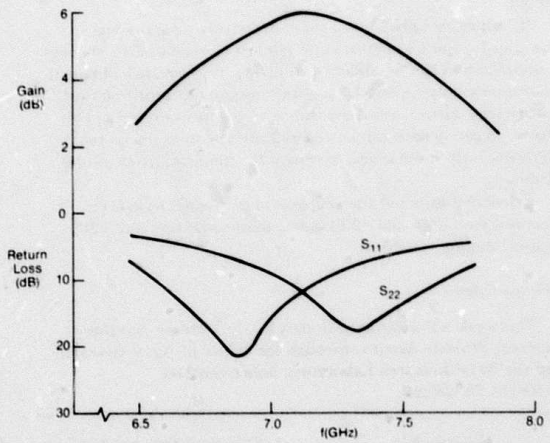

FIGURE 3–Gain and match vs frequency for monolithic amplifier, employing a 900μ directly implanted FET

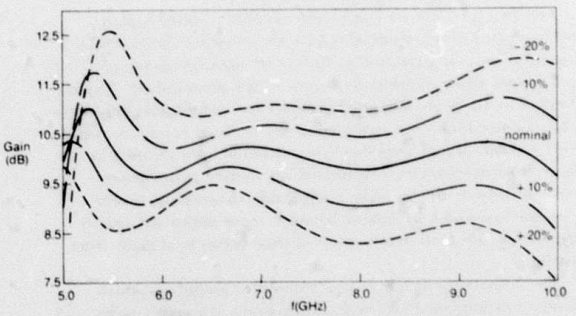

FIGURE 5–Frequency response as a function of gate length deviations from nominal.

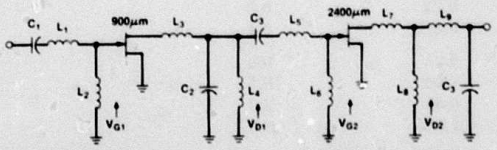

FIGURE 4–Two-stage monolithic lumped element amplifier.

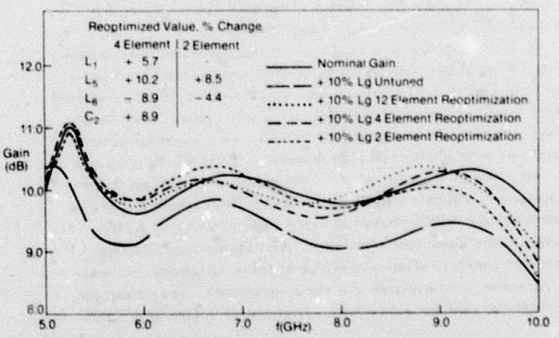

FIGURE 6–Amplifier response for various retunings to compensate for gate length 10% over nominal.

APPENDIX F

DESIGN CONSIDERATIONS FOR WIDEBAND MONOLITHIC POWER AMPLIFIERS

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One of the major problems encountered in designing wideband multistage FET power amplifiers is achieving the required 6 dB/octave/stage gain compensation over the band as well as maximum power output simultaneously. Reactive mismatching is commonly used to provide the required gain compensation, however, the severe mismatches created thereby complicate the design of interstage networks considerably. In hybrid amplifiers, this problem is overcome by routinely using hybrid coupled balanced amplifier pairs for each stage. To implement such an approach requires input and output quarter-wavelength directional couplers plus two parallel gain and phase matched amplifier stages. For monolithic amplifiers, such an approach is very wasteful of GaAs substrate area, particularly for frequencies below 10 GHz.

An alternate technique has been developed which distributes the gain equalization among input, interstage, and output stages. This alternate approach is based on load-pull characterization of the devices and may be summarized as follows:

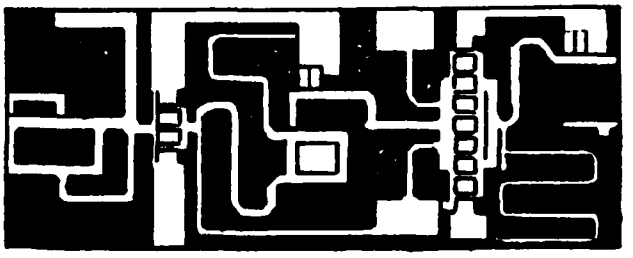
1. For a given fixed input power level, load pull contours are plotted corresponding to constant power output at each frequency.
2. The output circuit (or interstage circuit in the case of the first stage) is designed to present an impedance locus which crosses these constant power contours in a manner to provide constant power at each frequency.

Thus, the output circuit provides the optimum load impedance at the highest frequency of interest while selectively "de-optimizing" the load impedance at lower frequencies to provide constant power (and gain). An amplifier designed using this approach is shown below.

This "lumped element" amplifier incorporates a 900 μ FET in the first stage and a 2400 μ FET in the second. Matching circuits utilize interdigital capacitors and inductors formed by short lengths of transmission line and incorporate a trim capability. The first iteration of this amplifier produced ≃660 mW from 4.25-7.5 GHz with a peak power of .82 watts, and an associated nominal gain of ≃7 dB. A second interation employing circuit vias for improved source grounding (lower inductance) and increased circuit flexibility is in processing. Because of the lower inductance afforded by the vias, this improved version is calculated to have a minimum power output of 1 watt over the 5-10 GHz band. Experimental results will be presented at the symposium.

These amplifiers were fabricated at the Westinghouse R&D Laboratory, Pittsburgh, PA, under the direction of Drs. J. G. Oakes and M. C. Driver.

*This work was supported in part by the Defense Advanced Research Projects Agency, through the Office of Naval Research under Contract N00014-78-C-0268.



2 Stage 1 Watt Octave Bandwidth Amplifier

APPENDIX G

Publications

1. J.G. Oakes, M.C. Driver, R.A. Wickstrom, G.W. Eldridge, S.K. Wang, and E.T. Watkins, "Directly Implanted GaAs Monolithic X-Band RF Amplifier Utilizing Lumped Element Technology," 1979 GaAs Symposium Digest, p. 22, Lake Tahoe, Nevada, Sept 27-28, 1979.

2. J.E. Degenford, M. Cohn, R.G. Freitag, D.C. Boire, "Processing Tolerance and Trim Considerations in Monolithic Amplifiers," 1980 ISSCC Symposium Digest, p. 120-121, San Francisco, Cal., Feb. 13-15, 1980.

3. J.E. Degenford, R.G. Freitag, D.C. Boire, M. Cohn, "Design Considerations for Wideband Monolithic Power Amplifiers, 1980 GaAs IC Symposium Digest, p. 22, Las Vegas, Nev., Nov. 4-6, 1980.

4. V.L. Wrick, J.X. Przybysz, M.C. Driver, S.K. Wang, E.S. Coleman, R.A. Wickstrom, and J.G. Oakes, "Fabrication Considerations for Multistage Monolithic Power Integrated Circuits," 1980 GaAs IC Symposium Digest, p. 38, Las Vegas, Nev., Nov. 4-6, 1980.

5. J.E. Degenford, D.C. Boire, R.G. Freitag, M. Cohn, "A Study of Optimal Matching Circuit Topologies for Broadband Monolithic Power Amplifiers," 1981 Int'l MTTS Symposium Digest, p. 351-352, Los Angeles, Cal., June 15-19, 1981.

Contract Reports

1. Technical Report for the Period 15 March 1978 - 15 September 1978, NR 251-028, June 1979.

2. Technical Report for the Period 30 September 1978 - 31 March 1979 and 31 March 1979 - 30 September 1979, NR 251-029-10, January, 1980.

3. Final Technical Report for the Period 1 October 1979 - 31 July 1980, NR 251-029-3, December, 1980.

APPENDIX H

Publications of Consultants to Contract N00014-78-C-0268

(I) IEEE Transactions on Electron Devices, Vol. ED-27, No. 6, June 1980, 1045

PHYSICAL AND MATERIALS LIMITATIONS ON BURNOUT VOLTAGE OF GaAs POWER MESFET's

by Sandip Tiwari, Student Member IEEE, Lester F. Eastman, Fellow, IEEE and Lynn Rathbun

Abstract

This paper presents a study of factors limiting the burnout voltage of GaAs power MESFET's. A new device geometry had been investigated. Novel techniques using electron-beam induced current (EBIC) in the drain loop in a scanning electron microscope (SEM) and the shift in carbon Auger line in a scanning Auger microscope (SAM) have been applied to study the bulk electric field distribution and the surface voltage distribution. These techniques have been used to identify the regions of high electric field that lead to device burnout. The highest burnout voltages were observed at 8×10^{16} $.cm^{-3}$ doping with at least 60V burnout at full channel current and 85V near pinchoff conditions. This is a new state of the art.

An optimum undoped buffer-layer thickness is observed to be compatible with high burnout voltage and low leakage current. Finally, under optimized conditions of doping and geometry, no improvement is observed in the burnout voltage with the use of a higher doped contact layer.

(II) Electronics Letters 27th September 1979, Volt. 15, No. 20

EFFECTS OF ION IMPLANTATION ON DEEP LEVELS IN GaAs

by T. R. Jervis, University of Nevada, D. W. Woodard and L. F. Eastman, Cornell University

Abstract

We have studied the effects of ion implantation in GaAs using the techniques of deep-level transient spectroscopy. Samples included an unimplanted epitaxial buffer layer, a sample implanted directly into that buffer layer and then capped with Si_3N_4, a sample implanted into

that buffer layer through a similar cap, and a sample implanted directly into a semi-insulating substrate and then capped. All implants were with Si^{29} and both types of implant were annealed at 860°C for fifteen minutes. We find that the total density of deep levels is not changed significantly by direct implantation, capping and annealing but that implantation through a cap greatly increases the total deep-level concentration. Deep levels found in implanted layers after capping and annealing are primarily characteristic of the substrate or buffer layer into which the implantation is made, unless the implant is through a cap in which case contaminants from the capping process may be evident at high densities.

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